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VOLUME 5 NUMBER 5
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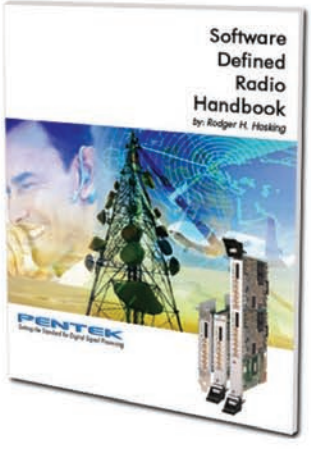

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July/August 2009 Volume 5 Number 5

COLUMNS

DEPARTMENTS

ON THE COVER:
Based on an exclusive interview with General Dynamics, editor Sharon Schnakenburg tells how the Army's WIN-T enables mobile comms via the DoD's Global Information Grid (GIG). General Dynamics has successfully built and tested the largest mobile network of its kind, providing an environment in which commanders at all echelons will have the ability to maneuver anywhere on the battlefield and communicate and collaborate with warfighters, command posts, and analytical centers at remote locations throughout the battlespace. Story on page 18. (Image courtesy of General Dynamics C4 Systems; www.gdc4s.com)

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Reflective memory speeds shared access applications

By Duncan Young

The introduction of network-enabled applications to many defense and aerospace projects allows multiple participants to work cooperatively with shared data. Using file servers and Network Attached Storage (NAS), the applications can access and update the same data sets wherever they might be located on the network. Ethernet is the first choice of network technology for military and commercial/office applications of this type. However, there is a class of applications where Ethernet or other network/fabric technologies are just not fast or deterministic enough. Flight simulators, aircraft simulators, jet engine testing simulators, or war gaming/battlefield simulators are typical examples of complex systems requiring significant amounts of distributed computing power, sometimes spread over quite large distances and sharing large arrays of volatile data in real time. Many of these applications have turned to reflective memory because of its low latency and high degree of determinism.

Reflective memory principles

The basis of reflective memory operation is its ability to autonomously replicate the contents of one processor's memory to the memory nodes of all other network members. As a processor writes to memory, the location and content are propagated around a network to the same addressable location in all other network memory nodes. It is not necessary for the processor that is writing data into memory to use any protocol for the replication to take place; however, at the system level there is a need for some predetermination of ownership and access rights to locations within memory space. But this allocation is entirely user- or application-dependent. Higher layers of protocol such as semaphores or handshaking can be added, but again, only if required by a particular application's needs.

A typical application for reflective memory might be an aircraft simulator with processing nodes representing sensors, communications subsystems, flight systems, cockpit display systems, and so on. A number of these nodes would be writing data onto the network, which then replicates the data to all the other nodes. For example, a sensor node, such as a weather radar, will generate a stream of data representative of that particular sensor type, varying in real time with the attitude of the aircraft as it flies through the simulation scenario. With many sensor types and many subsystem types feeding data into such a distributed processing application, it is vital that latency and system response mirror the real-world environment for the simulation to be truly representative.

Low latency

Keys to the success of reflective memory are its low latency and determinism. Using reflective memory, the typical node-to-node propagation time is on the order of 1 microsecond. Thus, in a system of 30 nodes, it would take only 30 microseconds to propagate through the network to all nodes. Data is transferred at rates up to the available network bandwidth, which can be 170 MBps or more. Achieving the same latency using other network technologies, such as Ethernet, is impossible even using datagram broadcast because of IP protocol overheads, addressing, and memory write times.

Ring topology

Reflective memory networks use a high-bandwidth, ring topology with commonly used 2.12 Gbaud signaling to move data in dynamically variable packets of 4 to 64 bytes. Such a ring will have its own data transmission protocols and error checking/recovery mechanisms plus optional managed hubs, if required, to bypass faulty nodes. The network can be easily expanded simply by adding more memory nodes as required. Using fiber as the network media, node-to-node transmission distances up to 300 m using multimode fiber are possible, or up to 10 Km using single-mode fiber. Reflective memory appears as just a block of memory addressed by its host processor via PCI or PCI Express, enabling it to be used in heterogeneous processing systems with many different host and operating system combinations that support PCI or PCI Express. An example of such a reflective memory node with up to 256 MB of SDRAM, suitable for attachment to a host processor via PCI Express, is the PCIE-5565RC from GE Fanuc Intelligent Platforms (Figure 1).

Figure 1 | The PCIE-5565RC reflective memory node from GE Fanuc Intelligent Platforms.

Both large-scale aerospace/industrial simulators and smaller embedded simulators found within battle groups across a number of vehicles can benefit from the speed of response provided by reflective memory. Currently, no other technology offers the same levels of latency and determinism for use in high-performance, widely distributed, shared data processing applications.

To learn more, e-mail Duncan Young at young.duncan1@btinternet.com.

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COTS vendors speed FPGA development cycle

By John Wemekamp

Although FPGAs are now used for DSP in many very diverse applications, they have become indispensable when parallel and repetitive algorithms are required by surveillance, Signals Intelligence (SIGINT), and Electronic Counter Measures (ECM) applications. In military guise, often operating over extended environmental ranges, these applications require the high channel count, I/O bandwidth, high performance, low latency, and small size that only an FPGA-based product can provide. However, the complexity and inherent flexibility of today's devices require prequalified tools, IP components, and a coherent development framework to keep tight project control and achieve realistic time-to-deployment goals. COTS vendors are rising to the challenge of developers' maturing expectations by continuously improving toolsets and product integration.

The case can be so strongly made in favor of using FPGA-based technologies for military sensor processing that the key decision point is now between using internal resources or buying off-the-shelf. Decision makers should weigh factors including time-to-market, the availability of the necessary in-house skills, the cost of training, and the level of risk. Additional consideration should be given to the potential return on investment, which might be measured in size, weight, or power saved, reduced recurring cost, selling in greater quantities, or enhanced competitive differentiation. However, in the defense and aerospace market, production volumes are often small with limited opportunity for direct reuse elsewhere, highlighting the need to keep development cost and risk to a minimum.

Integration

Because of its many benefits, the FPGA can become the focus of attention when selecting the sensor's overall architecture. It is relatively straightforward to visualize, simulate, and scale the DSP problem to the proposed sensor application using high-level tools such as The MathWorks' Simulink. But equally important is integrating the FPGA with the overall system environment: data acquisition, buffering, internal/external memory control, data path bandwidth, results dissemination, synchronization, error recovery, fault reporting, instrumentation for test and verification, and, finally, proof of operation over the platform's temperature extremes. This mix of internal, external, and interface issues to be resolved will require close integration of tools, libraries, I/O modules, and vendor-supplied IP. When forming part of a heterogeneous processing system, an FPGA must also be integrated with other processor types using common I/O, data structures, and middleware to abstract the detail of differing hardware implementations. Using a switched fabric such as Serial RapidIO is a key element, and vendors are now offering faster, lighter Serial RapidIO IP, prequalified over temperature, targeted to the needs of military DSP architectures.

System-on-Chip

The capacity, performance, and highly optimized DSP algorithms of the latest FPGA generations make them better able to support an open standards-based SoC infrastructure. Some of these available standards are AMBA, Wishbone, and OpenFPGA. All have the common objectives of offering a comprehensive set of device-agnostic architectural features and facilities to create a framework that supports the development of customers' application IP. Much of the IP support offered by COTS vendors today will be of value in the development of tested and qualified SoC ports for their future hardware products.

I/O flexibility

Typical off-the-shelf embedded systems, in form factors such as CompactPCI, VMEbus, or newer VPX (VITA 46), offer FPGA-based solutions in a variety of basecard and mezzanine formats. The recently introduced FMC (VITA 57) mezzanine standard adds flexibility by providing a small, optimally sized module for high-speed signal capture with multi-GHz serial signaling to baseboard-mounted FPGAs. This small form factor makes an FPGA and FMC mezzanine ideal partners for specialized I/O tasks such as protocol or media conversion, legacy communications, and digital video processing.

Many military sensors must operate over extreme temperatures. Because of the high power dissipation and GHz+ signaling of a typical large FPGA (10 W to 18 W), thermal design of hardware becomes critical because temperature sensitivity becomes very difficult to identify and diagnose later. Qualified and characterized off-the-shelf modules and tailored IP mitigate these risks and can significantly reduce a project's overall development time. One such qualified module is the FPE320 from Curtiss-Wright Controls Embedded Computing (CWCEC). Shown in Figure 1, it supports both the largest Xilinx Virtex-5 FPGA device types and offers the I/O flexibility of an FMC mezzanine site in the 3U VPX air- or conduction-cooled form factor.

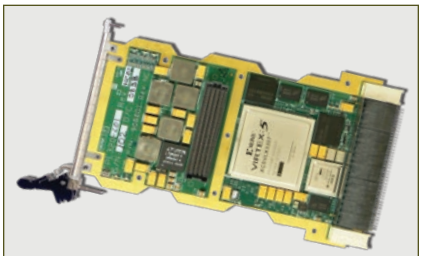

Figure 1 | The FPE320 supports both the largest Xilinx Virtex-5 FPGA device types and offers the I/O flexibility of an FMC mezzanine site in the 3U VPX air- or conduction-cooled form factor.

The promise of significant size, weight, power, and recurring cost reductions continues to stretch developers' resources to achieve their initial development cost and time targets. Considerable gains are possible by using COTS vendor-supplied hardware modules, IP cores, libraries, and drivers. Consequently, this has been proven an effective strategy by many contractors.

To learn more, e-mail John at john.wemekamp@curtisswright.com.

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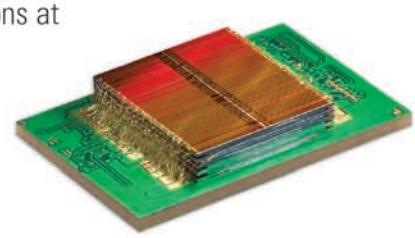

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Legacy Software Migration

By Mark Pitchford

Legacy enhancement: Nightmare or dream?

It can be a real nightmare when a customer wants a new solution based upon legacy software for which the original developers left no clear indication of design criteria. But finding the proper analysis methodologies and tool suites can help developers get a good night's rest.

Leafing through most sales brochures for software test tools, anyone could be forgiven for thinking that all software projects begin with a blank sheet of paper, a clear set of design criteria, and ample time to design and develop the ideal solution.

In reality, most development work involves the enhancement of existing code, all too frequently developed by a series of application gurus who have left the company and were more keen on getting something working than maintaining documentation or adhering to coding standards.

Avoiding false dawns

So what kind of nightmare unfolds when an order hinges on such Software of Unproven Pedigree (SOUP) acquiring enhanced functionality? Or worse: What if requirements dictate that modern coding standards need to be retrospectively applied to it (such as JSF++ AV, MISRA-C:2004, the CERT C Secure Coding Standard, or even internal company rules)?

Some software testing products suggest that they can find all your software errors simply by deploying mathematical techniques to predict dynamic behavior through static analysis. It sounds like a dream come true. After all, it saves the developer from rethinking/revamping current programming practices, never mind past ones. However, as in the rest of life, if something sounds too good to be true, it probably is. Such an approach can find some specific runtime errors such as division by zero or out-of-bounds array accesses, and if that is all that is required then it might be a winner. But the false warnings raised are likely to soon lead to sleepless nights in a cold sweat.

Even if it is true that a few runtime errors can be found, the resulting solution has to be proven from a functional perspective, too. No static analysis approach can do that. So, the danger of never finding the errors based on what is required is beyond

doubt a significant nightmare. Customers will not pay, devices are deployed without complete testing, and the specter of what lies behind the unintelligible warnings could haunt the soundest sleeper.

Given that the analysis of dynamic behavior by static means is of limited use, what else is there? What of the better-established dual-pronged approach of sound coding standards coupled with the dynamic analysis of code by execution? Does that really demand a *green field* application with an idealized development path to become a dream solution?

Heading out of the darkness

In an effort to change the nightmare into a dream even when the starting code has no complete, written specification, developers need to start with the specification for any amendments and let the original source code simply define the existing behavior. So, the trick is now to capture that existing behavior and ensure that it *only* changes where change is demanded by the incoming order, even if the new project demands a higher coding standard.

Some dynamic test tools provide just such a point of reference by statically analyzing the source code. The knowledge gleaned is then used to automatically generate unit tests to create a *personality profile* of the behavior of each existing method or function. Groups of functions can provide a similar role where modularity is not the order of the day. By generating such unit tests on the original code and exercising them on the revised sources, it is possible to ensure that behavior has only changed where change is required.

Although this *personality profile* approach has merit and makes sleep a little easier, issues remain. For instance, it assumes that the original source code is sound because the application has been proven in the field. But what if some of the new functionality builds on software code that was rarely used there? And even the well-proven parts of the code are likely to now be handling very different data. How will they behave?

Studies indicate that software submitted to only functional testing and field applications is still likely to have code that remains unproven. Dynamic test tools highlight unproven or rarely used execution paths, and static analysis tools help isolate areas that are vulnerable to the newly introduced data sets and in need of more testing. When that work is complete, the *personality profile* tests established at the outset are modified to provide a regression test set both to prove the current phase and to ease the path for any additional development work.

In the military world, thanks to enforced DO-178B standards, few nightmare applications are quite this unsettling. However, projects do exist where at least some elements of this extreme scenario ring true. So, it is useful to know which methodologies and which tool suites provide the means to address each of these issues. Prudent, careful use of these proven techniques can yield the results you dream of.

Sleep well.

Mark Pitchford *has more than 25 years' experience in software development for engineering applications, the majority of which have involved the extension of existing code bases. He has worked on many significant industrial and commercial projects in development and management, both in the UK and internationally including extended periods in Canada and Australia. For the past seven years, he has specialized in software testing and works throughout Europe and beyond as a field applications engineer with LDRA. He can be reached at Mark.Pitchford@ldra.com.*

Daily Briefing: News Snippets

By Sharon Schnakenburg, Associate Editor

www.mil-embedded.com/dailybriefing

April's showers produce more than May flowers

Semico's most recent report on semiconductor sales indicates a case of revenue turnaround – at least when contrasted with ongoing gloomy forecasts. While industry pundits predict a semiconductor sales decline of 20 to 30 percent for 2009, Semico predicts only a 12 to 13 percent 2009 revenue decline in light of "overall market softness." Semico president Jim Feldhan's rationale is derived from what he describes as a quarterly cyclical trend, where the final month of any quarter produces significant sales surges. This, he says, inevitably relegates the following month to a sharp comparative decline. Situated in this tenuous position, April has historically seen this decline range between 17.2 percent (in 2004) and 34.8 percent (in 2001) in comparison with March sales. The silver lining for April 2009 materialized in the form of a "record" low sales decline: only 7.6 percent in comparison with March 2009. Meanwhile, industry strongholds for 2009 are forecasted to include GPS systems, netbooks, and HDTV, among others.

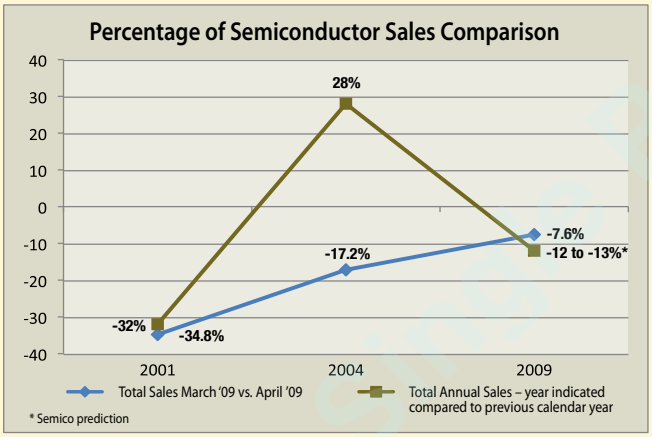


Figure 1 | Semico predicts only a 12 to 13 percent 2009 revenue decline in light of "overall market softness."

RoboScout to enlist in the German military

The more lives that can be spared on the battlefield by using unmanned technology, the better, as implied by the German Military of Defense's new RoboScout project. Presently in the development stage, prime Base Ten Systems Electronics GmbH (Base10) will incubate the modular Unmanned Ground-based Vehicle (UGV), earmarked to handle multiple roles including reconnaissance, SIGINT, support of satellite and terrestrial/radio data links, and aiding other vehicles' communications by serving as a relay station. To facilitate said communications transmissions while proffering deterministic messaging, high reliability, and real-time low-latency performance, Real-Time Innovations (RTI) will provide its Data Distribution Service middleware. The middleware features a publish-subscribe model and is predicted to ease RoboScout's future expansions and upgrades.

Military technology meets the "Terminator"

Some philosophers theorize that life imitates art, but does art imitate – or utilize – technology? Yes, in the case of the recently released "Terminator Salvation" movie, where a triad of Crystal Group Inc.'s real-life military technology wares appear in the movie's command center workstation: the rugged RS47F and RS234T servers, along with the RD2217 rugged display. Crystal Group's immortalized military offerings are tough enough to take on the same extreme environmental threats depicted in celluloid, according to the company, presumably even Skynet's nuclear annihilation. Proving the point is the RD2217, a rugged dual 17" 2U EIA display, which meets MIL-STD-810F's operational temp (0 to +55 °C), storage temp (-55 °C to +85 °C), altitude (12,500 ft operation; 40,000 ft transport), and vibration (5 GRMS, 5-500 Hz, 75 min/axis) requirements (with vibration kit).

Coast Guard software hastens search

When Air France Flight 447 recently fell into the Atlantic Ocean, French authorities knew they needed to recover passengers and crew, flight wreckage, and the aircraft's data recorders as quickly as possible. Assisting in the sobering endeavors was the U.S. Coast Guard, whose efforts were hastened with its Search and Rescue Optimal Planning System (SAROPS) software system. SAROPS predicts a search area by analyzing floating wreckage locations in conjunction with wind, weather, and sea conditions during a specified time period to estimate a plane's likely location. SAROPS – developed collaboratively by Northrop Grumman, Applied Science Associates (ASA), and Metron, Inc. – additionally accesses data from radar, satellites, models, and in-situ observations to allow SAR controllers to rapidly examine probable scenarios. As of press time, Flight 447's precise crash locale is not yet determined and its data recorders are still missing, perhaps laying somewhere within the identified 77,220 square mile (200,000 square km) search area: approximately the size of Nebraska state.

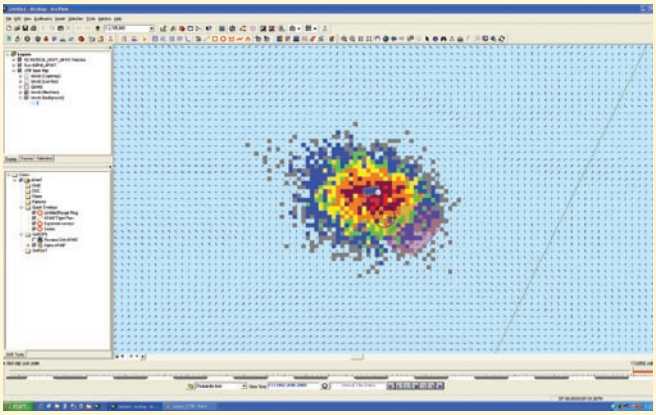


Figure 2 | SAROPS search and rescue technology, figure courtesy of Applied Science Associates (ASA).

Pilots preview their future before it happens – with 100% availability

Many people would love to live in or view their own future before it happens – and without the possibility of any lasting consequences. Though time travel isn't a reality just yet, the F-15E Mission Training Center located in Suffolk, England might be the next best thing. A joint project of prime The Boeing Company and the U.S. Air Force, the center – in operation since April 2008 – recently ascended to the "100 percent availability" milestone. Giving military pilots in training the chance to fight before they actually face the real world, the center contains a duo of high-fi, dual-cockpit F-15E simulators. Each simulator is equipped with a cutting-edge visual system providing realistic 360-degree visuals within a synthetic environment. The simulators' 3-D imagery, rendered by Quantum3D Inc.'s Independence image generator, flies by at 60 Hz. To date, the center has supported 400-plus training missions.

Figure 3 | The F-15E Mission Training Center located in Suffolk, England recently reached "100 percent availability" (photo courtesy of Boeing)

Radar breaks new ground ... kind of

Though a recent contract between a U.S. Army agency and Curtiss-Wright Controls Embedded Computing's (CWCEC's) 3d-Radar group has been described by company officials as "groundbreaking," ironically CWCEC's summoned Ground Penetrating Radar (GPR) technology works *in advance of* breaking any ground. Under the agreement, CWCEC will provide its GeoScope and B3231 antenna technologies for the primary purpose of detecting Unexploded Ordnances (UXOs) and other buried objects. The Army's version contains enhancements including the GeoScope's "real-time view," which provides operators the capability to see post-processed GPR data – within mere milliseconds of data's initial acquisition. Detection algorithms from Exponent, Inc. were integrated with the real-time view, and deliveries to the U.S. Army are expected through March 2010.

AMD's Radeon: In less-familiar territory

A prevalent contender in PC markets, AMD is now soaring into the embedded safety-critical avionics industry with its ATI Radeon E4690 GPU – empowered by ALT Software's DO-178B-certifiable 2D/3D OpenGL drivers. The ATI Radeon E4690 renders in excess of 3x the ATI Radeon E2400 embedded graphics accelerator's performance. The ATI Radeon E4690 also provides a PCI-E 2.0 x16 interface, along with 512 MB on-chip memory and a 128-bit memory interface. Meanwhile, ALT Software, Wolf Industrial Systems, and Channel One recently announced their Advanced Graphics Solutions (AGS) Group, which aims to develop end-to-end technology tailored around the ATI Radeon E4690 graphics accelerator.

Platform readies C4ISR technologies

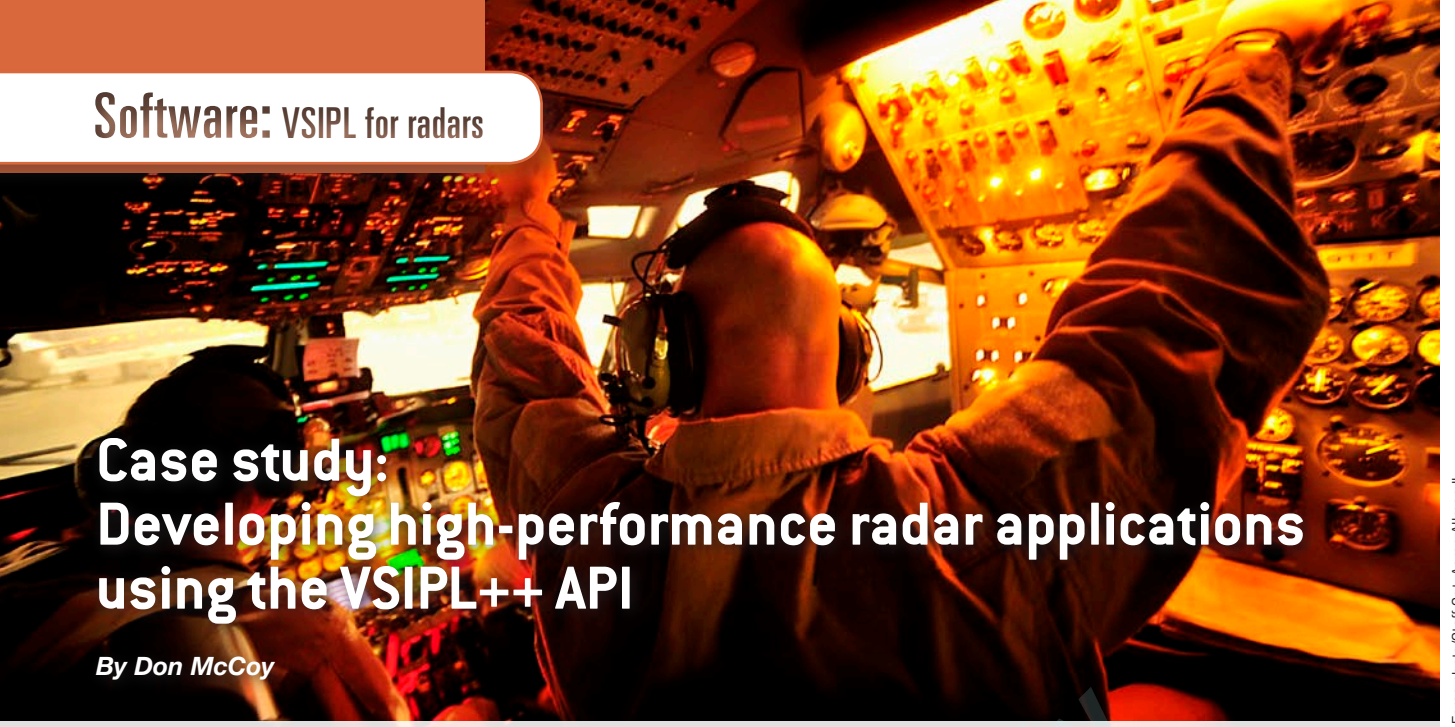
Ensuring warfighter success is contingent upon effectively developing, testing, and fielding deployable wares to the battlefield. One proof of concept is Lockheed Martin's Airborne Multi-INT Laboratory (AML), which renders a platform for researching, testing, and demonstrating new C4ISR capabilities, to prepare for future deployment (Figure 4). AML will aid in investigation of emerging Reconnaissance, Surveillance, and Target Acquisition (RSTA) methods, in addition to facilitating the development of an operational concept touted to link all echelons' battlefield resources. Anticipated experimentation exercises consist of improving end-to-end intelligence, beginning with the initial concept and proceeding to sensor cross-queing, exact geolocation, and finally, fast transmission to end users. Additionally, AML's Service Oriented Architecture (SOA)-based architecture enables reach-back to other databases and information sources and accommodates cyber security schema integration.

Figure 4 | AML photo courtesy of Lockheed Martin

Satellite to provide insight for smartphone-size devices

Space Systems/Loral's (SS/L's) well-traveled TerreStar-1 satellite has come a long way – and is still on the move (Figure 5). First, it was launched from the European Spaceport in French Guiana onboard an Ariane 5 rocket. Next, its first thruster firing transpired in early July, with the goal of propelling TerreStar-1 to its final geostationary orbital locale at 111.0 degrees West longitude. The final goal: The satellite's 18-meter antenna reflector, designed for umbrella-like unfolding once it gets to its orbital slot, will facilitate video, data, and voice transmissions to smartphone-sized mobile devices utilizing a 2 GHz spectrum. The progeny of SS/L's joint effort with Hughes Network Systems, TerreStar-1 includes a Ground-Based Beam Forming (GBBF) system that can direct the satellite's power where it's most needed at any given time. TerreStar-1 can generate spot beams over the continental U.S., its territories, and Canada.

Figure 5 | TerreStar-1 photo courtesy of Space Systems/Loral



Case study: Developing high-performance radar applications using the VSIPL++ API

By Don McCoy

U.S. Air Force photo/Staff Sgt. Aaron Allmon II

The challenge was to implement high-performance Synthetic Aperture Radar (SAR) for two platforms in one week.

The need for high-performance Signal- and Image-Processing (SIP) applications is driving interest in parallel and multicore hardware for military embedded systems. However, programming such complex architectures can increase development costs by reducing developer productivity and code reuse. Leveraging a library that implements the high-level VSIPL++ API provides a way for SIP software developers to take advantage of the performance potential of parallel and multicore hardware systems while satisfying schedule and cost constraints.

The problem: Getting from prototype to high-performance production code efficiently

Consider the following challenge. A software developer has a Scalable Synthetic Aperture Radar (SSAR) benchmark expressed in 50 lines of MATLAB code. The developer needs to implement that benchmark to achieve good performance on two very different systems – a conventional x86 processor and a heterogeneous, multicore Cell Broadband Engine (Cell/B.E.) processor – in just one week.

For background, Synthetic Aperture Radar (SAR) is used for a variety of imaging and remote sensing applications, including reconnaissance, surveillance, and terrain mapping. To standardize benchmarking this common algorithm, MIT Lincoln Laboratory created a scalable synthetic SAR application as part of the High Performance Embedded Computing (HPEC) Challenge[1]. The benchmark demonstrates the intense computational requirements found in actual systems using synthetic (and scalable) data. The raw radar returns are processed by means of a 2D Fourier matched filtering step, a spatial frequency interpolation step, and a transformation back to the spatial domain. Key mathematical operations, as in any SAR application, include FFTs, matrix multiplication, and interpolation. Thus, a software development technique that offers benefits for this SSAR's benchmark points to an approach that is likely to work for larger SIP applications as well.

The first step: Choosing a library-based solution

If high performance were the only goal, the developer could consider coding the algorithm in a low-level language such as C or assembly code. But the time constraints (only a week), combined with the need to develop for both an x86 and a Cell/B.E. processor, make this approach unworkable.

With a portable library, though, the same application code will run on more than one system. And a library allows a developer to program for an unfamiliar architecture, such as the Cell/B.E., in a familiar language using familiar development tools. The key is to find a library at the right level of abstraction – high enough to provide the necessary primitives for the application domain but low enough to allow for efficient implementations and thus high performance.

For the SSAR benchmark, the VSIPL++ API provides the right level of abstraction. VSIPL++ is an open standard[2], high-level API for parallel high-performance signal and image processing. It is defined by the High Performance Embedded Computing Software Initiative (HPEC-SI – www.hpec-si.org), a consortium of industrial, academic, and governmental partners, with sponsorship from the Air Force Research Laboratory. Its goal is to simultaneously deliver productivity, portability, and performance. VSIPL++ defines a pure C++ interface for operations – including FFTs, filters, linear system solvers, and other mathematical functions – that allow SIP applications to be written at the problem domain level.

For the SSAR benchmark challenge, CodeSourcery used Sourcery VSIPL++, a library that provides an optimized implementation of the VSIPL++ API on x86, Power Architecture, and Cell/B.E. processors with useful extensions to the base VSIPL++ specification.

The next step: Implementing SSAR in VSIPL++

Using the VSIPL++ library, CodeSourcery implemented SSAR in C++ in just four days. To illustrate the relative advantage of the VSIPL++ API for developer productivity, Figure 1 shows three different implementations of the SSAR algorithm's fast time filter: (1) MATLAB, (2) simple, unoptimized C[3], and (3) VSIPL++. Mathematically, they all perform the same computation, but the VSIPL++ version, like the MATLAB version, is easy to understand because it is expressed in SIP primitives such as FFTs and matrix multiplication.

MATLAB

```
# Filter echoed signal along fast-time
sFilt = fft( sRaw ) .* ( fastTimeFilter * ones(1,mc) );

# Compress signal along slow-time
sCompr = sFilt.* exp(ic*2*(ks(:)*ones(1,mc)) ...
      .* (ones(n,1)*sqrt(Xc^2+(-ucs).^2)) – ic*2*ks(:)*Xc*ones(1,mc));
```

C

```
ftx2d(S,Mc,N);

for(i=0;i<N;i++) {
  for(j=0;j<Mc;j++){
    tmp_real=S[i][j].real;
    tmp_image=S[i][j].image;
    S[i][j].real=tmp_real*
      Fast_time_filter[i].real-tmp_image*Fast_time_filter[i].image;
    S[i][j].image=tmp_image*
      Fast_time_filter[i].real+tmp_real*Fast_time_filter[i].image;
    }
  }

for(i=0;i<N;i++) {
  for(j=0;j<Mc;j++){
    tmp_value=2*(state->K[i]*(sqrt(pow(Xc,2)+pow(Uc[j],2))-Xc));
    cos_value=cos(tmp_value);
    sin_value=sin(tmp_value);
    fp[i][j].real=S[i][j].real*cos_value-S[i][j].image*sin_value;
    fp[i][j].image=S[i][j].image*cos_value+S[i][j].real*sin_value;
    }
  }
```

VSIPL++ Setup

```
Matrix<complex_t> s_compr_filt(…);

s_compr_filt = vmmul<col>(fast_time_filter,
    exp(complex_t(0, 2) * vmmul<col>(ks, nmc_ones) *
        (sqrt(sq(Xc) + sq(vmmul<row>(ucs, nmc_ones))) - Xc)));

col_fftm_type ft_fftm(Domain<2>(n, mc), 1);
```

VSIPL++ Compute

```
// Filter echoed signal along fast time and compress
s_filt = ft_fftm(s_raw) * s_compr_filt;
```

Figure 1 | The VSIPL++ implementation of the SSAR fast time filter, like MATLAB, is much more compact than the unoptimized C.

Ignoring the setup of the filter coefficients, the VSIPL++ version of the fast time filter requires a single line, performing two data-parallel operations sequentially. By contrast, the C reference implementation is more verbose and thus more error prone. In addition, because the C code is iterative, it is more difficult to divide among multiple processors or to optimize for different architectures.

The C and VSIPL++ implementations were benchmarked on both a conventional Xeon processor running at 3.6 GHz and a Cell/B.E. processor running at 3.2 GHz. The entire front-end processing chain was run looping over the data 10 times to average out the measurements. On the Xeon platform, the VSIPL++ library used the Intel Performance Primitives (IPP) library v5 and Intel Math Kernel Library (MKL) v7.21 as well as FFTW v3.1.2. On the Cell/B.E. platform, the VSIPL++ library used the Cell Math Library v1.0 and FFTW v3.2-alpha3. The VSIPL++ code needed no changes to run on both architectures; the VSIPL++ library utilized these underlying math libraries without explicit direction from the developer.

Because development costs vary roughly linearly with the number of lines of code, it is important to look at performance and Source Lines Of Code (SLOC) count together to understand the relationship between developer effort and performance benefit. Here, the VSIPL++ version offers both productivity and performance

improvements over the C reference implementation on two very different processors. The VSIPL++ version requires 48 percent fewer lines of code and achieves speedups of 68x and 146x on the Xeon and Cell/B.E. platforms, respectively. Tables 1a and 1b show the source line counts and performance of the VSIPL++ and C implementations of the core 2D Fourier matched filtering and interpolation routines.

The VSIPL++ approach offers particular advantages on the Cell/B.E. processor because it relies on the VSIPL++ library's implementation of the SIP primitives. Several of the primitives used in the SSAR algorithm, such as two-dimensional FFTs and the matrix multiplication operations used for filtering in the frequency domain, are computationally intensive and also involve significant data movement to and from the eight Synergistic Processing Elements (SPEs) of the Cell/B.E. processor. Getting good performance from the SPEs requires carefully balancing the input and output of data with the computations being performed. Optimizing a C implementation to achieve comparable performance would greatly increase program complexity and thus would drive up development time and cost.

Table 1a: SLOC

	MATLAB	Unoptimized C	VSIPL++
Matched Filtering	24	109	17
Interpolation	22	76	23
Setup/Other	4	206	163
Overall Total	50	391	203

The extra mile: Unlocking hardware's potential with strategic optimization

Finally, opportunities for optimization were investigated in the VSIPL++ implementation for the Xeon and Cell/B.E. processors. For example, in the fast time filter computation (see again Figure 1), the VSIPL++ code performs an FFT followed by a matrix multiplication. Given large enough data sets, memory accesses in the second step cause cache misses on a Xeon processor,

Table 1b: Performance

	Unoptimized C		VSIPL++		Optimized VSIPL++	
	Xeon	Cell/B.E.	Xeon	Cell/B.E.	Xeon	Cell/B.E.
Matched Filtering	13.6 MF/s	4.5 MF/s	1.57 GF/s	29.6 GF/s	3.17 GF/s	30.6 GF/s
Interpolation	23.2 MF/s	7.9 MF/s	1.12 GF/s	0.4 GF/s	1.13 GF/s	5.6 GF/s
Overall Total	16.9 MF/s	5.6 MF/s	1.15 GF/s	0.8 GF/s	1.71 GF/s	9.9 GF/s

Tables 1a and b | SLOC vs. performance: VSIPL++ requires 48 percent fewer lines of code than C and yet runs 68 times faster even on Xeon.

leading to expensive reads from main memory. Rewriting this loop so that each row is processed one at a time (that is, taking the FFT and then performing the vector multiplication) results in a 1.6x speed improvement for this portion of the code. The change is trivial to implement, requiring only a net increase of eight lines of code, yet it yields a *20 percent* improvement in the execution time of the entire front-end stage.

On the Cell/B.E. processor, profiling reveals that interpolation takes almost 40 times longer than matched filtering. A large amount of time is spent in a loop over data in the "range" direction (perpendicular to the flight path), performing a polar-to-rectangular coordinate conversion. A contribution from several inputs for each side-lobe of the sinc function used in the interpolation is added to calculate the intensity and phase of the corresponding output pixel. This computation cannot be expressed well using VSIPL++ primitives.

To improve performance, CodeSourcery used a VSIPL++ API extension available in Sourcery VSIPL++ called "user-defined kernels." User-defined kernels allow the developer to write a high-performance computational kernel and still leverage the data-handling aspects of the VSIPL++ library. A hand-coded kernel with 208 lines of code speeds up interpolation from 4.23 seconds to 0.18 seconds, an improvement of more than 23 times that of the original implementation.

On Xeon, the final optimized code runs more than 82 times faster than the C reference implementation. On the Cell/B.E., it was 5.7 times faster than on the Xeon and more than 1,400 times faster than the reference C code. Even modest, easy-to-implement changes can significantly improve performance.

Combining performance, productivity, and portability with VSIPL++

Using a library implementing the open-standard VSIPL++ API made possible the development of a complex application in far fewer lines of code than are necessary in C. Out of the box, this code outperformed the C reference implementation. With limited changes to address performance bottlenecks, performance was further enhanced. And the application remained portable across vastly different architectures.

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General Dynamics and WIN-T: Pursuing the GIG

Figure 1 | Increment 2's development testing, paired with Increment 3's technologies maturity evaluation, was held September through December 2008 at Fort Huachuca, Arizona. (photo courtesy of General Dynamics)

By Sharon Schnakenburg, Associate Editor

Much like the constantly on-the-move soldiers it aims to inform and protect, the Global Information Grid (GIG) and its technological components never seem to stand still. One example is the U.S. Army's GIG-enabling Warfighter Information Network-Tactical (WIN-T) communications/networking program, with its always-moving, ever-evolving technologies.

WIN-T forms the network infrastructure of the U.S. Army's section of the GIG. "It's the equivalent of what you would have in, say, your data closet in an office building," explains Bill Weiss, vice president tactical networks for General Dynamics C4 Systems. WIN-T networking gear can be embedded into combat vehicles and installed in tactical communication assemblages, and provides broadband Internet, information services, and telephone services to command posts from theater through company levels.

Meanwhile, WIN-T's ever-evolving "increments" (see Sidebar 1), hardware and software components, and ties to the Army's new FCS transition depot – the Brigade Combat Team (BCT) Modernization Strategy – are what make it intriguing.

A B C and D of WIN-T increments

Increment 1: Also referred to as the Joint Network Node; provides network services to command posts at the halt; now deployed to more than half the U.S. Army.

Increment 2: Provides a mobile networking capability "so a commander has access to information ... even if he's in his vehicle moving along at 60 mph," details Bill Weiss, vice president tactical networks for General Dynamics C4 Systems. Ultimately will include more than 2,000 nodes and service 10 divisions and 40 brigade combat teams[1]. Development testing occurred September through December 2008 at Fort Huachuca, Arizona (Figure 1). Limited user tests were completed in March 2009.

Increment 3: Delivers mobile networking capability with improvements on Increment 2, including airborne relay capability and upgraded satellite and line-of-sight radio communications in a smaller package; limited user testing anticipated in 2011.

Increment 4: A long-term upgrade program to integrate bandwidth from the TSAT program, and more. (TSAT is on SECDEF Robert Gates' proposed budget's cutting board, however.)

Sidebar 1 | WIN-T's fourfold increments

Hardware and software composites

Weiss says Increment 2 features specialized network radios optimized for mobile use with their logical counterparts – omnidirectional beamforming antennas – to facilitate line-of-sight communications established on an ad hoc, as-needed basis. A built-in navigation system and satellite pointing mechanism are key.

Networking gear additionally consists of oft-ruggedized, off-the-shelf switches and routers. Prime contractor General Dynamics – whose WIN-T team members include Lockheed Martin and Program Executive Office Command, Control, and Communications Tactical, among others – sometimes partners with commercial vendors Cisco and Juniper Networks to create smaller routers when space is limited. (See Table 1 for a list of additional WIN-T suppliers.)

Meanwhile, WIN-T's software blends off-the-shelf and custom programs. Commercial software is used for network services, commercial routing, and commercial network management. Proprietary software is created for the specialized waveforms and automation necessary for supporting the mobile network.

Ties into FCS and BCT modernization strategy

WIN-T Increment 3 is the first WIN-T increment associated with FCS – which is now transitioning into what the Army calls its Brigade Combat Team Modernization Strategy – utilizing JC4ISR embedded radios and designed to meet FCS vehicle SWaP requirements. Though SECDEF Gates has put all except the initial FCS increment on the proposed chopping block, General Dynamics continues with its various WIN-T increments – undaunted.

WIN-T embedded systems suppliers and wares
Wavestream's solid-state amps
Cisco's Unified Communications Manager Software
General Dynamics' GoBook XR-1 computer
TRAK Microwave Corporation's Modular Time Code Processor
Network Equipment Technologies, Inc.'s NX1000 multiservice networking platform
Expand Networks' Accelerator Operating System
Netcordia's NetMRI network change and configuration management tool

Table 1 | These are just some of the companies providing their wares to one or more WIN-T increments.

[1] The government classifies one mobile node of WIN-T Increment 2 possessing a TCN, POP, and SNE.

Finding the right balance: Deep packet inspection encourages innovation and information sharing while protecting DoD networks

By Kevin Curran

Faced with growing network usage, the DoD can look to deep packet inspection to differentiate authorized, unauthorized, and recreational traffic at a deeper level for better security, bandwidth management, and overall information assurance.

U.S. Air Force photo by Senior Airman Levi Riendeau

Modern warfare places very particular requirements on network communications infrastructure. As the Department of Defense (DoD) evolves to support a net-centric environment, the agency's networks are critical to maintaining the secure collaboration and information sharing necessary for a common operational picture of the battlefield and mission operations.

Yet DoD networks also support a wide range of traffic that is not mission critical. With a growing pool of next-generation converged applications, like VoIP and streaming multimedia, unauthorized and recreational use of the network increasingly occupies the bandwidth needed for vital mission operations. In addition to placing a heavy strain on defense networks, this high volume of unauthorized network traffic conceals malicious content from security tools.

The inherent threat posed by a larger user population along with a greater appetite for mission-critical information means that the DoD needs to fully understand and manage who is on the network, what users are doing, and the resources to which they have access. DoD network administrators must look beyond legacy network analysis methods toward the implementation of Deep Packet Inspection (DPI) technologies to keep the agency's networks reliable, timely, and secure.

DoD threats, both foreign and domestic

According to informal estimates, 70 percent of DoD network traffic is deemed "unofficial." This means that traffic unrelated to DoD business is largely dominating the agency's available bandwidth, diminishing the throughput available to conduct and support missions, and harming network security.

For example, streaming media websites like YouTube are particularly troublesome for DoD networks. Often quite large, these files can create asymmetric traffic flows that lead to bandwidth problems. Independent analysis of DoD network traffic finds that use of such streaming media websites peaks during high-profile events such as the NCAA March Madness tournament and the Olympics.

Needless to say, this recreational use of bandwidth poses a very real threat to national security. In fact, a recent DoD report to the Senate Armed Services Committee on DoD personnel access to the Internet highlighted that, if left unchecked, unauthorized and recreational use of DoD networks can leave less bandwidth available for, and even obstruct, mission-critical data transfers. In addition, and frankly even more problematic, by creating an even higher volume of traffic, recreational use potentially camouflages and allows intruders, viruses, and other malicious threats to masquerade as benign traffic. According to a report to Congress on DoD Personnel Access to the Internet[1], Peer-to-Peer (P2P) traffic, like music file sharing from Kazaa, can be especially dangerous since it often introduces corrupt files to the network and can elude traditional security tools.

Recent observations of the DoD's inbound network traffic indicate that the overwhelming majority is associated with ports typically related to Web traffic, which are outlined in Table 1. By itself, this association does not imply that the traffic is legitimate.

Common TCP/IP Port Numbers

Port Number	Application
Port 21	FTP File Transfer
Port 25	SMTP E-mail Delivery
Port 80	HTTP - Internet Traffic
Port 110	POP3 Mail Delivery and Collection
Port 143	Remote E-mail Access (IMAP4)

Table 1 | The majority of traffic inbound to the DoD is associated with these typical Web ports, but this association does not imply that the traffic is legitimate.

In fact, oftentimes this traffic represents malicious activity that simply "disguises" itself as legitimate Web traffic. Cyber-related attacks on agency networks increased 158 percent in 2007, according to the Department of Homeland Security (DHS), and disguised traffic is likely in part responsible for this sharp uptick. Considering this very real and growing threat, the DoD must eliminate the potential for recreational network use to contribute to potential security lapses.

As an example of efforts underway to tackle the network security and bandwidth challenge, the Defense Information Systems Agency (DISA) put in place

the Global Information Grid – Bandwidth Expansion (GIG-BE) program to increase bandwidth and diversify physical access to approximately 87 critical sites in the continental United States. The DoD also blocks access to popular recreational websites such as YouTube, MySpace, and Photobucket on official military computers in the battlefield.

While these proactive efforts help improve network reliability, some of the methods are limited, at best, in their capabilities. What is needed are DPI-enabled applications that offer richer visibility into the traffic traversing the network.

DPI: A policy-centric approach to a net-centric challenge

To protect the integrity of DoD networks and ensure sufficient bandwidth for essential operations, administrators must determine the exact nature of the traffic consuming network bandwidth, as well as block or prioritize traffic with network-wide policy enforcement. What's more, detection and analysis must take place without compromising network speed or adding latency.

Through standard Transmission Control Protocol (TCP)/Internet Protocol (IP) networking, data is sent between systems using small packets that quickly traverse the network and are reassembled at the respective end points to recreate the original information. The purpose of current traffic monitoring and management technologies is to scan the individual data packets to detect specific patterns, issue alerts about attacks or unauthorized use, and block harmful activity.

For instance, common security applications include Intrusion Detection Systems (IDS), Intrusion Prevention Systems (IPS), and firewalls. Firewalls are generally used to block harmful traffic at Internet ports or suspect IP addresses. Many modern-day firewalls can also identify and block harmful protocols. While firewalls inspect both inbound and outbound traffic, they only provide protection at the deployment site, do not protect the network at the fourth through seventh levels of the Open Systems Interconnection (OSI) model, and also do not articulate policies to determine rights of access. Figure 1 illustrates the additional visibility offered by DPI-enabled technologies.

DPI-enabled devices, on the other hand, permit the transfer of extremely large amounts of data at wire speed while giving unprecedented visibility into deeper levels of network traffic to identify and remedy security vulnerabilities and unauthorized use.

Operating at layers two through seven of the OSI model, DPI-enabled applications can direct, filter, and log IP-based applications and Web traffic, regardless of the protocol or application type, by searching for defined protocol-specific characteristics such as URLs for http or an e-mail address for SMTP in the data's "DNA." These variables are configured by the network administrator in a rules or policy engine that implements those polices according to signature-based comparisons; heuristic, statistical, or anomaly-based techniques; or some combination of these. For example, many DPI devices can identify packet flows (in addition to conducting a packet-by-packet analysis), allowing the implementation of control actions based on accumulated flow information.

By nature, DPI applications require definitions of each applicable protocol in

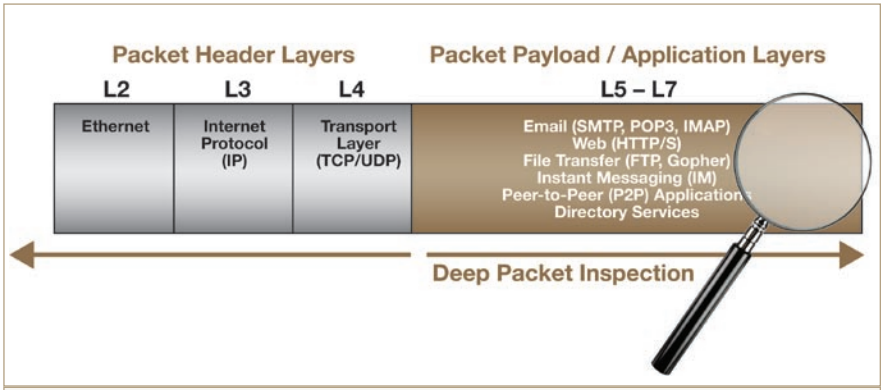

Figure 1 | DPI goes beyond the surface layers of the OSI model to view the actual contents of each data packet.

order to operate. Thousands of Ethernet protocols exist, each with their own unique session format. Moreover, these protocol definitions change frequently due to modifications from standards groups or the introduction of new protocols. While many L4 security devices only examine the IP header of a data packet to identify the IP and port information before making packet-handling decisions, DPI systems can solve greater packet processing challenges due to a more comprehensive examination of data protocol and characteristics.

Purpose-built DPI platforms can combine the functionality of an IDS, IPS, and firewall as well as any other DPI-based applications (that is, those for lawful intercept and data leakage prevention), thus delivering significant additional features and protections to allow network administrators to streamline and secure traffic flow. A message tagged as "high priority," such as a mission-critical communication, can be routed to its destination ahead of low-priority messages or packets involved in recreational activities such as viewing sports highlights or listening to streaming radio. The deeper level of visibility also means that malicious data associated with unauthorized use can be identified and acted upon. This capability is essential to combating the challenges presented by recreational or unauthorized use of military networks.

A common operational platform for network management

DPI-enabled appliances enhance the capabilities of traditional security, traffic management, and network monitoring and analysis solutions. Ideally, the DoD should look to deploy these technologies on one common operational platform leveraging both internally developed Government Off-the-Shelf (GOTS) applications and Commercial Off-the-Shelf (COTS) applications. The network devices must keep pace with multi-gigabit line rates and support real-time deep-packet processing.

To satisfy the requirements for DPI, a platform must be:

- Linux-based, as a majority of forward-leaning security and network monitoring applications are open source and Linux-based
- Customizable to accommodate ever-changing network solutions requirements
- Cost-efficient, since physical space, facilities, and power costs force the DoD to make budget-conscious, high-performance decisions
- Programmable so the DoD can rapidly develop, deploy, and manage mission-critical operations, new services, and applications
- Policy-centric, allowing the DoD to define its own policies for network traffic
- IPv6 supported, since the government has mandated the adoption of Internet Protocol version 6 (IPv6) this year

Meeting the DoD's vision of a secure and robust network supporting all information classification levels and collaboration requires unique network analysis and control capabilities. Supported by a flexible platform and comprehensive policies, DPI-enabled applications surpass traditional security tools to provide an unprecedented level of visibility for sound bandwidth and security controls. Ultimately, this technology can help the DoD find the right balance between encouraging communications and innovation while also protecting the security and integrity of DoD data.

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MIL/COTS DIGEST

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In This Issue

The changing face of SBCs

For years, the largest number of new embedded products crossing our desks were SBCs on 6U-sized LRUs. That stands to reason, since nearly every system needs one of them – usually stuck in a VME backplane's Slot 1. But the advent of processors bolted to mezzanine cards such as PMC or XMC, in addition to the new VITA 59 System-on-Module (SoM) specification, has fragmented the market a bit. We're now receiving new processor type products that don't resemble the traditional 6U SBC of yore. And even more interestingly, we're seeing more sensor mezzanine cards where the CPU of choice – essentially also making them "SBCs" by definition – is not a processor at all. Instead, most mezzanines now include an FPGA engine into which hard- or soft-core CPUs are embedded.

Herein you'll find 19 new-to-us, hand-selected VME-related products in this "All About VME" *MIL/COTS DIGEST* supplement. Not all form factors are strictly VME, though. You'll find: 2 "traditional" VME SBCs, both equipped with Core 2 Duo Intel CPUs, along with 1 PowerPC-based VPX SBC and a VITA 59 SoM also with a Core 2 Duo. There are 2 Ethernet boards or switches, in VPX and optional CompactPCI versions. Depending upon how you slice it, there are 3 to 5 PMC, XMC, and FMC (FPGA mezzanine card) modules here – most of which include high-res A/D front ends supplemented by Altera Stratix II or Xilinx Virtex-5 FPGAs. Finally, we've included a handful of chassis (including one that's mist cooled) and a backplane ready to accept VME64, VPX, or CompactPCI boards. All in all, this *MIL/COTS DIGEST* provides a great cross-section of the evolving VME ecosystem.

Chris A. Ciufo, Editor

3U VPX Ethernet switch

The VPX6-683 FireBlade switch provides a fast, secure approach to interconnect subsystems, chassis, cards, and compute nodes in platforms using 1 and 10 GbE links. It comes in 3U VPX VITA 48.2 air- and conduction-cooled rugged versions, equipped with a fully managed or unmanaged switch/router with 24x 1 GbE SERDES ports (IEEE 802.3) and 2x 10 GbE uplink/stacking ports (XAUI). Providing up to 24 wire speed 1,000 Mbps interfaces and up to 2x 10 Gbps interfaces in a single 3U VPX slot, the VPX6-683 is ideal for architecting system-wide Intra-Platform Networks (IPNs). The VPX6-683 FireBlade also features high-performance Layer 2/3+ switching/routing software, along with management ports including Serial RS-232 and in-band GbE. The switch is additionally outfitted with a Rear Transition Module (RTM) with SFPs for 1 GbE and InfiniBand connectors for 10 GbE.

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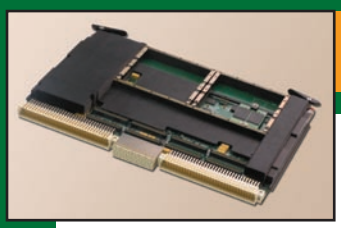
Extended-temp 6U VMEbus CPU

The Maritime VS275 is a 6U VMEbus CPU (one- or two-board set) that enables seamless upgrades and extensive flexibility with the addition of five different expansion modules. It utilizes the GMS P70 Nucleus processor module, which supports either the ultra-low power Core 2 Duo operating at 1.5 GHz (L7400 @ 17 W) or the Core 2 Duo at 2.16 GHz (T7400 @ 34 W) with 4 MB of L2 cache and 667 MHz FSB. "Plug-in" configurability is provided, and custom configurations are possible through one PMC-X and/or 16-lane XMC compliant site(s) with rear I/O plus an optional workstation I/O module (second VME site). Meanwhile, I/O comprises three PMC-X sites and/or two eight-lane XMC sites and one PMC-X site; or two Special Application Module (SAM) video modules – one with dual-link DVI-I and one with dual DVI-I to the front panel – and one PMC-X site. Maritime VS275 supports VME 64 and is available in a standard temperature range of 0 °C to +60 °C or an extended temperature range of -40 °C to +85 °C.

www.gms4sbc.com — **GENERAL MICRO SYSTEMS, INC.**



Low-power, high-performance 6U VME SBC

Aitech Defense Systems' C160 is an air- or conduction-cooled 6U VME SBC featuring the Intel T7500 low-power or high-performance Merom Core 2 Duo dual-core processors. It offers clock frequencies up to 2.2 GHz for the high-performance version and 1.67 GHz for the low-power version, which draws only 25 W. The SBC offers 2eSST and 2eVME functionality as well as VME and PCI legacy support via a Tundra Tsi148 bridge. C160 provides up to 2 GB fast DDR2 SDRAM operating at 667 MHz and up to 8 GB of onboard flash disk (NAND flash) with IDE controller. The SBC also features an integrated GM965 graphics engine with 2D and 3D graphics outputting in either CRT (RGBHV) or composite NTSC, PAL, or RS-170 video formats. It additionally offers two industry-standard PMC sites, two GbE ports, two SATA II interfaces, and two USB 2.0 interfaces, plus legacy interfaces such as two 16C550-compatible RS-232/422/485 serial ports and eight discrete I/O lines.

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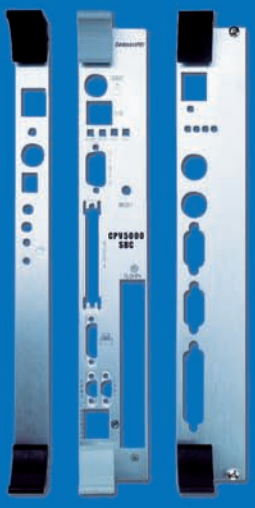

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Adopting VITA 57 (FMC): Reducing FPGA I/O headaches

By Ron Huizen

No longer just a "sea of gates," FPGAs are now used in just about every type of application you can think of, giving COTS designers the ability to solve myriad problems by using the same board in various systems. The solution isn't always a simple one though, as FPGA I/O requirements vary from system to system. However, the VITA 57 (FMC) standard comes to the rescue with its unprecedented mechanical and electrical flexibility. Meanwhile, IP and interoperability are also vital considerations.

Sometimes a design team will see a really nice COTS FPGA board that was just about perfect for their application – if only that front panel interface were 12 V instead of 3 V, or round instead of square, blue instead of red, or some similar tweak. Engineers who have experienced this scenario are going to love VITA 57 (FPGA Mezzanine Card or FMC). The reason: VITA 57 provides a standard specification for a small mezzanine module designed to adapt an FPGA-based carrier card to different I/O requirements.

Prior to this standard, most vendors were developing their own proprietary mezzanine boards or redesigning them to fit necessary I/O stipulations – a much more costly equation. However, the FMC specification aims to thwart these costly and time-consuming practices by providing a COTS standard for the industry. However, VITA 57 has its share of plusses and challenges. Primary areas of consideration for FMC use and development include mechanical and electrical details, and FPGA IP – along with the issue of whether you'll really be able to put an FMC from one vendor onto the FMC site of another vendor.

Introducing FMC

The FMC is defined as a small add-on module to provide physical-level I/O drivers for carrier cards with FPGAs. (Also see Sidebar 1 for nonstandard uses of FMC.) Carrier form factor support includes VME, VXS, VPX, CompactPCI, and AMC.

Nonstandard uses and extensions for FMC

While FMC was designed to provide I/O for FPGAs, a nonintended use is to provide additional processing, whether it be another FPGA or a DSP. With 10 W allowed, and more as long as you can cool it, FMCs could be used to enable what are essentially coprocessors for the baseboard FPGA.

Another nonstandard use of FMCs is in full-size AMC modules, where one has much more height available. For example, while Small Form-factor Pluggable (SFP) cages cannot fit within the standard FMC component envelope, in a full-size AMC, one could put the SFP cages on the back side of the FMC. Note that this approach can also be used on other form factors, but requires an additional slot – not optimal for deployment but often suitable for prototyping.

Sidebar 1 | In addition to its targeted advantages and purposes, FMC can also provide some nonstandard benefits.

The underlying factor driving FMC is the complexity, and hence time and cost, inherent with developing large FPGA boards conforming to the latest industry standards, whether they be communications focused like AMC or more military-centric such as VPX. Given this complexity, there are several benefits to be gained by allowing these boards to be more easily adapted to different customer requirements with a smaller and much simpler I/O module.

This simpler VITA 57 add-on module allows customers to use the same baseboard for different applications, thus providing the advantages of using a common platform, including all of the associated development tools and supporting software. Vendors can more easily customize their COTS offerings, which should result not only in savings for the customer due to lower Non-Recurring Engineering (NRE) costs, but also in a wider choice of available boards. Finally, customers themselves could become proficient in developing their own FMCs, allowing them to focus on their specific I/O while taking advantage of COTS base boards. An example FMC is shown in Figure 1.

FMC mechanicals

Mechanically, the FMC is about half the size of a PMC, at 76.5 mm (deep) by 69 mm (wide), with an I/O depth of 31 mm. With the default stacking height of 10 mm, component envelopes are 4.7 mm

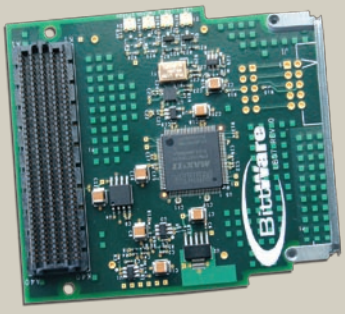


Figure 1 | A VITA 57 add-on module allows customers to use the same baseboard for different applications.

below and 1.3 mm above, with the I/O area allowing for 9.5 mm. Using an optional 8.5 mm stacking height, designers can move 1.5 mm from below to above. The front panel has a PMC-like bezel, though slightly (12.95 mm) narrower. FMC also includes support for conduction cooling.

The small size of the FMC could be a challenge for some applications. With a front-panel bezel narrower than PMC and so many signals available, it will be difficult to find connectors that maximize the full advantage of the FMC signals (see Electricals section). However, allowing for larger FMCs would have meant giving up more precious space on the carrier boards, so the standard attempts to strike a reasonable balance.

To help address this issue, VITA 57 defines a double-wide FMC. As is the case with double-wide PMCs and AMCs, however, we don't expect to see very many of these double-wide FMCs on the market. Double-wides tend to be used in specific programs that need the extra real estate and don't require as much modularity or compatibility with different carriers.

FMC electricals

Using a Samtec SeaRay high-speed connector, FMC supports up to 10 multi-gigabit lanes, 80 differential pairs (or 160 single ended), clocks, JTAG, and I^2C. The connector comes in low (160) and high (400) pin count versions, with the standard providing mappings for both.

For power supplies, FMC mandates 3.3 and 12 V, along with an adjustable (0-3.3 V) voltage. Maximum current on the three supplies is 3, 1, and 4 A respectively, though the module is limited to 10 W of total power.

FMC IP

FMC provides a standard way of adding different physical-level I/O devices directly to a carrier board's FPGA. This means FPGA IP needs to be developed in the FPGA to deal with these I/O devices. Along with the IP, there will usually need to be some form of control software.

Whereas other mezzanine modules such as PMC usually have onboard control and talk to a standard interface like PCI, there is no standard interface for FMCs because they are designed to tie directly to the carrier's FPGA pins. It's expected that a vendor providing both the FMC and the carrier board would develop and provide this IP, but it still must be done, and, of course, takes time and money. It's also expected that some FMC vendors will provide IP cores for interfaces to their modules, but they still need to be integrated into the carrier board's FPGA. This issue has not gone unrecognized within VITA; consequently, there is a working group in progress discussing it.

Interoperability: Mixing FMCs and carriers from different vendors

Perhaps the largest challenge with FMCs results from the flexibility that VITA 57 provides. With so many available signals and even an adjustable voltage supply, making sure an FMC will work on a carrier will not be as easy as with previous mezzanine modules like PMC, which had a standard PCI bus interface. The VITA 57 standard provides guidelines for mapping signals and for carriers and modules with respect to advertising features and requirements, but designers should expect to have to do some legwork

when selecting FMCs and carriers. The specification itself contains a 38-question compatibility checklist as an appendix.

Even if designers find that there is indeed a match between the module and carrier, they still need to develop, or at least port, the FPGA IP and control software for the carrier, as mentioned previously.

For straightforward FMCs – for example, a fiber-optic conversion module that just connects to some multi-gigabit lanes – it should be possible to mix and match between vendors. But for complex modules, it might not be so easy. But is this really a problem? In perception, yes, but in marketplace realities, perhaps not. One would not really expect many companies to be in the business of selling just FMCs; it's more realistic to expect that carrier vendors will develop some FMCs that mate to their carriers and allow their customers to develop their own. Another possibility is that engineering design services firms start gaining expertise in FMCs and bridge this gap.

VITA 57 meets FPGA I/O flexibility requirements

FMC provides a standard method for COTS board vendors and their customers to more easily extend and adapt their standard FPGA-based products. The specification provides a lot of I/O flexibility in an attempt to meet many differing requirements, while also balancing the needs of the carrier and mezzanine. Although there might be some interoperability and IP challenges with FMC, it at least provides a method to allow for potential compatibility and reuse where previously there was none. Several VITA 57 modules and carriers have already been announced. BittWare is following suit, putting FMC sites on its new Altera Stratix IV based AMC (Figure 2) and VPX boards and will soon begin developing FMC modules.

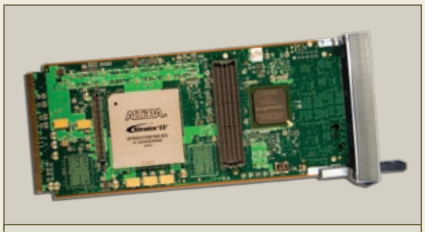


Figure 2 | Vendors such as BittWare are putting FMC sites on their boards. Pictured: An Altera Stratix IV based AMC.

Ron Huizen *is vice president of technology at BittWare. Before joining BittWare, Ron held various roles in electronic product development at Amirix Systems. Prior to Amirix, he worked at Nortel Networks for several years on SS7 switching systems. He holds a Bachelor of Computer Science from Acadia University in Wolfville, Nova Scotia, and a Master of Computer Science from Carleton University in Ottawa, Ontario.*

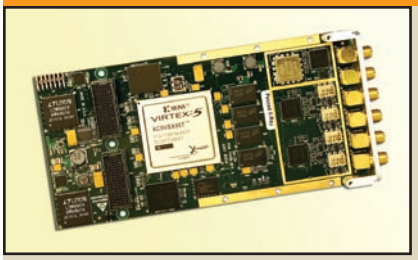
BittWare
603-226-0404 • www.bittware.com

Ultra-rugged 3U VPX CPU board

Kontron's VX3230 is a 3U VPX CPU board offering scalable performance with high bandwidth over the backplane for ultra-rugged defense and aerospace applications. It is powered by a Freescale 1 GHz MPC8544 32-bit PowerPC processor and is ultra-low power for dedicated processing tasks, affording power output of less than 10 W. VX3230 combines the fundamental strengths of the VMEbus architecture, such as robustness and excellent EMC, with the new high-bandwidth capabilities of the VPX connector for high-speed differential signaling over the backplane. Available in a Rugged Conduction-cooled (RC) version, the CPU board supports operational temperatures from -40 °C to +85 °C. It also includes up to 1 GB of DDR2 RAM, along with 2x GbE ports configurable on either the front or the back, dual SATA-150 ports, two USB 2.0 ports on the rear, an optional XMC/PMC slot for application-specific I/O expansions, and temperature sensors.

www.kontron.com **KONTRON**

PCIe XMC module for EW apps



Suitable for Electronic Warfare (EW) apps and more, the X5-TX is a PCIe XMC module (75 mm x 150 mm) that features four 500 MSps or dual 1 GSps, 16-bit DACs. It is powered by a Virtex-5 SX95T or LX155T FPGA with 512 MB DDR2 DRAM and 4 MB QDR SRAM. Also provided are four 500 MSps or two 1 GSps 16-bit DACs, along with ±1 V, 50 ohm, DC or AC coupled inputs and external or internal sample clocking and triggering. Eight RocketIO private links at 2.5 Gbps each are included, as is a >1 GBps, eight-lane PCI Express host interface. Additional capabilities include power management, wireless transmission, radar pulse generation, and high-speed arbitrary waveform generation.

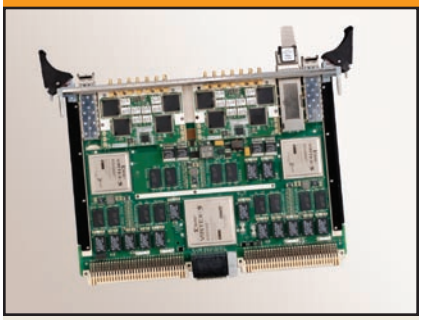
www.innovative-dsp.com **INNOVATIVE INTEGRATION**

MIL-STD-1553 modules for VME

The N7 and N8 modules provide MIL-STD-1553 functionality for VME, CompactPCI, and PCI multifunction boards. A library of functions provides the mix-and-match capability to configure a wide variety of functions on a single board, eliminating the complexity of using multiple, independent, single-function cards while reducing SWaP and costs. Other typical functions include A/D, D/A, S/D, D/S, LVDT/RVDT, DLV, ARINC 429/575, RS-422/485/232, discrete and TTL I/O, reference generator, differential transceiver, and RTD. Featured are two dual-redundant MIL-STD-1553B Notice 2 interface channels, and each channel can be configured to act as a Bus Controller (BC), Remote Terminal (RT), or Monitor (MT). Continuous BIT health monitoring is provided, and operating temperatures range from -40 °C to +85 °C and 0 °C to +70 °C.

www.naii.com **NORTH ATLANTIC INDUSTRIES**

6U VXS digitizer board



The Quixilica Atlas-V5 VXS is a 6U ANSI/VITA 41 (VXS)-compliant, high-speed digitizer board that combines high-density FPGA processing with four or eight 12-bit ADC input channels performing at 1 GSps. By employing three Xilinx Virtex-5 FPGAs, Atlas-V5 offers high FPGA processing density per channel, making it ideal for high-channel-count signal processing applications. Six digital I/O channels run at up to 3.75 Gbps using one QSFP and two SFP+ front-panel connections. In addition, rugged versions are available.

www.tekmicro.com

TEK MICROSYSTEMS, INC.

6U VME system enclosure

The Series 415 VME system enclosure for 6U X 160 mm (up to 340 mm) cards features side air intake with removable air filters, rear exhaust, and a cable way extending from the front card area to the inside rear panel. Series 415 has rugged aluminum construction and accommodates VME/VME64x, CompactPCI, and VXI backplanes. Many power options are provided, including dual-redundant hot swap. Other features include dual AC inputs, removable air intake filters, and voltage/fan monitors.

www.vectorelect.com

VECTOR ELECTRONICS & TECHNOLOGY, INC.

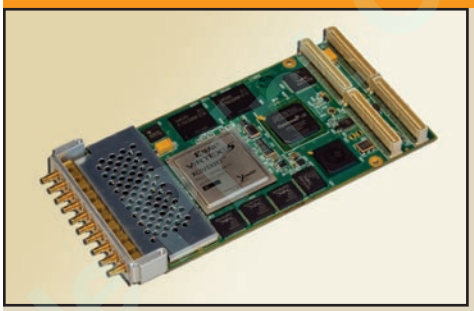
Field-upgradeable VME SBC

The NES-ILLUMINATOR is a 6U VME field-upgradeable VME SBC with a double-wide front panel based on COM Express modules. NES-ILLUMINATOR is available with Celeron M, Pentium M, Core 2 Duo, and Atom processors up to 2 GHz and up to 2 GB RAM. It includes a VME64 interface, along with five-row P1 and P2 VME connectors. Front-panel accoutrements consist of dual GbE channels with RJ-45, four USB 2.0 channels, and one DVI-I video port. The SBC includes an onboard CompactFlash slot, four PCI Express lanes on backplane connector P0, four USB 2.0 channels on backplane connector P0, and an optional user-programmable Altera Cyclone III EP3C40 FPGA. Other highlights are the PMC slot front and rear I/O access on P2, plus one FMC slot. Operating temperature is 0 °C to +70 °C or -40 °C to +85 °C.

www.nolam.com

NOLAM EMBEDDED SYSTEMS

VME/VPX ADC PMC module



The GE Fanuc ICS-1556B is an ADC PMC module. It is designed for demanding communication applications such as SDR, SIGINT, digital receivers, and tactical communications where analog data must be converted into digital information as close to real time as possible. Featuring an onboard Xilinx Virtex-5 SX95T FPGA, ICS-1556B also includes four 14-bit ADCs sampling synchronously at frequencies up to 400 MHz in addition to a 64-bit/133 MHz PCI-X interface. Signal processing capability provided by the FPGA allows the user to perform standard functions such as wideband Digital Down Conversion (DDC), Fast Fourier Transform (FFT), and time stamping – or to implement any required functionality. A Hardware Development Kit (HDK) provides support for users implementing their own FPGA signal processing algorithms, and ICS-1556B can be used with VME, VPX, PCI, and CompactPCI carrier cards.

www.gefanuc.com/embedded

GE FANUC INTELLIGENT PLATFORMS, INC.

VXS Virtex-5 FPGA digital receiver

The Echotek Series DCM-V5-VXS Virtex-5 FPGA digital receiver contains twin FMC modules equipped with two each of the following ADCs: 16-bit 130 MSps ADC converters, 14-bit 250 MSps ADC converters, or 10-bit 1.5 GSps ADC converters, with other options available. Meanwhile, FPGA choices include three Xilinx Virtex-5 SX240T or LX330T FPGAs. Additional highlights include DDR-II SDRAM and QDR-II SRAM and 3,156 DSP slices, along with multiple data paths between the FPGAs, FMC sites, and bidirectional VXS and RACE++ interfaces. The board supports the company's multinode coherency options, and DCM-V5-VXS's EchoCore firmware represents a library of FPGA cores, depending on the data processing required. The card set can also be ordered without the FMC modules under the name SCFE-V5-VXS.

www.mc.com

MERCURY COMPUTER SYSTEMS, INC.

Programmable VME resistance simulator

The V420 is a programmable resistance simulator. Each channel has an isolated DC power supply and digital interface, resistance simulation circuitry, signal conditioning, and input protection circuits. An internal microprocessor manages all data I/O and communicates with the VMEbus via a transparent, VMEbus-speed, dual-port memory. Relays are provided to connect any input channel to the dedicated D9 calibration connector for accurate four-wire verification of channel performance. Eight channels of fully isolated precision resistance/RTD simulation are provided, and V420 is resistance programmable from 5 ohms to more than 65 K in three ranges. It is also RTD-mode programmable for 100 R and 1 K platinum RTDs or 10 R copper RTDs.

www.highlandtechnology.com

HIGHLAND TECHNOLOGY, INC.

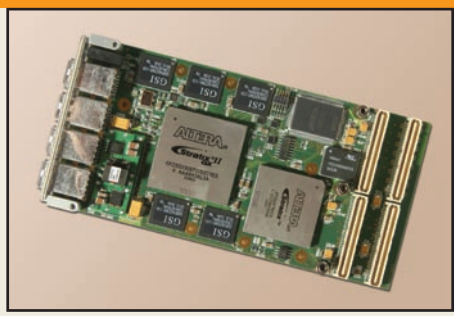
Rugged 3U VME direct-spray enclosure

SprayCool's MPE-3U is a rugged 3U electronics enclosure using direct-spray cooling technology. Target applications for the MPE-3U include sensor processing, electronic warfare, mission computing, and command and control for unmanned aircraft, helicopters, and ground-based vehicles. The enclosure has seven slots and upward, 3U orientation. It functions at altitudes up to 55,000 feet (75,000 feet optional) and at temperatures ranging from -55 °C to +71 °C (-65 °C optional). Power consumption is 80 W maximum for the cooling system, and input power is in compliance with MIL-STD-704 and -1275B; meanwhile, the enclosure is ruggedized to meet the MIL-STD-810F, -461, and -462 specifications. The MPE-3U chassis is also compatible with ½-ATR mounting standards and can accommodate a variety of customer-specified I/O and backplane options.

www.spraycool.com

SPRAYCOOL

Stratix II PMC module

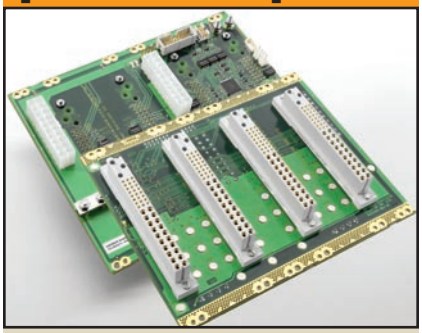


The PM432 is a PMC module implementing EP2SGX90 Altera Stratix II GX FPGA technology to provide a high-speed, high-bandwidth processing platform. PM432 is suited for SDR, WiMAX, radar, and video, as well as other computation- and bandwidth-intensive applications. PM432 includes 90,960 logic elements, 192 18 x 18 multipliers, and 4.3 Mb RAM, along with onboard nonvolatile storage of configuration data (two banks) and automatic configuration of FPGAs after power-up memory. As standard, five 512Kx36 (18 Mb) ZBT memories are afforded, while options include five 1Mx36 (36 Mb) ZBT memories. A peak PCI data rate of 533 MBps is supported, in addition to a sustained DMA data rate up to 420 MBps. PMC user I/O includes 64 user I/Os with LVTTL signal level (3.3 V), while front-panel I/O comprises four HSSDC2 connectors with up to 3.125 Gbps full-duplex bandwidth per connector. Serial RapidIO, Fibre Channel, GbE, and SerialLite II protocols are supported via the use of IP cores.

www.parsec.co.za

PARSEC

Intelligent VME power backplanes



Hartmann Elektronik's intelligent 4-Slot Power Backplanes are designed for VME and CompactPCI applications and feature an integrated, configurable microprocessor. The 4-Slot Power Backplanes provide capability for detecting the status of each power supply and reporting to the system by using the ACFAIL signal. Automatic control is additionally afforded if every power supply unit is properly inserted; moreover, all settings and addresses can be configured by using DIP switches. The 4-Slot Power Backplanes offer a current capacity up to 128 A and a temperature range of -40 °C to +85 °C.

www.hartmann-elektronik.de

HARTMANN ELEKTRONIK

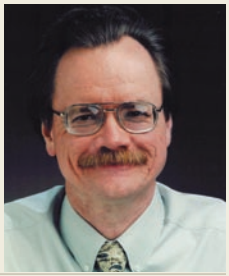
XMC network adapter

The XMC-GBX4 Ethernet is a quad GbE XMC that serves as a high-performance, low-latency network adapter. It provides four high-speed Ethernet interfaces with either front or rear access, in addition to up to four 10BASE-T/100BASE-TX/1000BASE-T ports with RJ-45 front connectors with status indicators. Up to four rear-accessible SERDES ports via Pn4 are also included, as are low-latency data handling and efficient packet prioritization for maximum system performance and throughput. XMC-GBX4 Ethernet supports Windows, Linux, and Solaris x86 and has VITA XMC-compliant interfaces for high bandwidth. Additionally, customization is welcomed, and extended availability is assured.

www.pinnacle.com

PDSi – PINNACLE DATA SYSTEMS, INC.

PICMG's xTCA meets VME and VPX head-on



EDITOR'S NOTE

Just when we think things might be settling down to a predictable level within VME's relatively stable ecosystem, our recent interview with Mark Overgaard, Pigeon Point Systems' founder and president, reveals otherwise. From the heretofore telecommunications-focused company's recent acquisition by Actel to its participation in OpenVPX, things are anything but predictable. Edited excerpts follow.

VME: ***Actel recently acquired Pigeon Point Systems. What did they see in your company?***

OVERGAARD: Pigeon Point Systems (PPS) was already using Actel's Fusion mixed-signal FPGA family as a base for our management solutions before the acquisition. Fusion's low power, live-at-power-up, and inherent reliability attributes make it a good fit for management controllers.

Since we additionally provide platform management products for PICMG's widely used Telecommunications Computing Architecture (or xTCA, to include both AdvancedTCA and MicroTCA), acquiring PPS brought Actel more expertise in platform management and customer relationships within the telecommunications sector.

VME: ***Tell us about "management," as you define it.***

OVERGAARD: Pigeon Point focuses on the layer of management closest to the hardware platform (which includes, for instance, a VPX chassis and the plug-in modules that populate its slots). We call this layer "hardware platform management"; it provides a foundation for upper management layers. Hardware platform management includes functions such as inventory data collection and thermal management.

VME: ***How does this apply to VPX?***

OVERGAARD: To maximize the benefits of COTS products in VPX applications, the VPX standards family needs to define platform management interfaces and functionality. This is needed so that system integrators can combine platform elements for their applications as quickly and efficiently as possible, while implementing the level of such management that is suitable for those applications.

We see two levels of platform management. First, there is local management at the module level that monitors sensors on the module and stores information about the module, such as inventory data. Second, there is chassis-level management that collects information from the modules in the chassis and represents the chassis to upper-level management.

VME: ***What are the challenges in mission-critical systems, particularly those based on VPX?***

OVERGAARD: One key challenge for hardware platform management in mission-critical systems is providing the right level of infrastructure services to fit the needs of the application. This is important because different applications and different system integrators might have very different views on how management should be partitioned between the application layers and underlying infrastructure layers. For example, some integrators consider most management functionality to be the responsibility of the application layer and prefer to embed that functionality there. We favor a tiered approach to VPX standards in this area so that module and chassis suppliers, as well as their customers, can choose the appropriate tier level for the management infrastructure layer while still gaining the interoperability and cost efficiencies that result from standardization.

For instance, there are likely 3U VPX modules that need only a minimal local management controller but must interoperate reliably with modules that have higher-tier (more sophisticated) local management. Actel's Protocol Design Services (PDS) group has proposed, within the VITA 46.11 working group, an approach to such minimal local controllers based on programmable logic devices such as flash-based FPGAs.

VME: ***What are the parallels between the traditional PICMG systems and VME-based aerospace and defense systems?***

OVERGAARD: Both VPX and xTCA define open modular platform architectures in which numerous companies participate (as developers, integrators, or both) and which depend on interoperability for the success of that ecosystem and the integrated systems it produces.

xTCA systems and the boards that populate them implement a rich and mandatory hardware platform management layer. The management layer of VPX architecture can benefit by leveraging the xTCA facilities wherever it makes sense for VPX – to take advantage of the significant investment that has already been made in the xTCA facilities. However, some aspects of xTCA platform management might not be needed in VPX, such as the extensive provisions for hot swapping boards.

VME: ***You're a member of OpenVPX. Why?***

OVERGAARD: The primary work of developing the VPX hardware platform management framework is occurring within VITA, and we're actively participating in that work as members of VITA. But you have to remember that the system-level architecture work OpenVPX is doing is an important complement to the work in VITA on a wide range of VITA 46 dot specifications. One of these is VITA 46.11, which covers hardware platform management within VPX. So we are members of OpenVPX to participate in the development of that system-level architecture.

Mark Overgaard *is founder and president of Pigeon Point Systems (PPS), now an Actel company. Mark is a leader on several PICMG technical subcommittees and also actively participates in defining VPX platform management. Prior to founding PPS in 1997, Mark was VP, Engineering at Lynx Real-Time Systems and Telesoft. He can be contacted at mark@pigeonpoint.com.*

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VITA 59 System-on-Module

MEN Micro's XM2 is an ESMexpress-based (VITA 59-based) System-on-Module (SoM) in a 95 mm x 125 mm form factor, featuring the latest Intel Core 2 Duo SP9300 processor with a clock frequency of up to 2.26 GHz. It is ruggedized for a variety of harsh, mobile, and mission-critical environments found in railway, avionics, and other applications. I/O includes four x1 or one x4 PCI Express links as well as two GbE ports, eight USB ports, three SATA ports, and one HD audio port. XM2 is equipped with 4 GB of DDR3 DRAM and USB flash on the carrier board, and its screened operating temperature is 0 °C to +60 °C (+32 °F to +140 °F) for both convection and conduction cooling. XM2 dissipates up to 40 W via the advanced fanless cooling system defined by the ESMexpress standard.

www.menmicro.com

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VME/VPX IPv4/IPv6 10 GbE switch

The ComEth4300a is an IPv4/IPv6 10 GbE switch. It is sold in the VME, VPX, and CompactPCI form factors and is manufactured by Interface Concept and distributed by ACT/Technico. The switch supports jumbo frames, full-wire speed Layer 2 bridging, and Layer 3 unicast and multicast engine forwarding, all running at full data rate. ComEth4300a also supports Layer 2 through Layer 4 advanced traffic classification, filtering, and prioritization. Its scope ranges from 24 to 28 ports, up to 4 of which can be 10 Gb. Additionally, automatic MAC address management, autonegotiation, autopolarity, and autocrossover are provided on each port, along with a routing capacity of 125 Million packets per second (Mpps). ComEth4300a switches come in standard, extended, and conduction-cooled grades, and an onboard, high-performance PowerQUICC III processor handles all management functions and protocol processing, including L3 routing and setup and additional L4 services.

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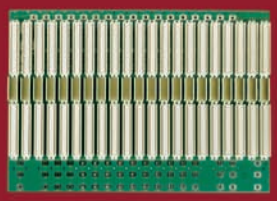
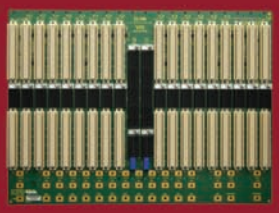
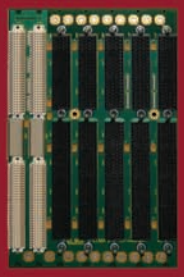


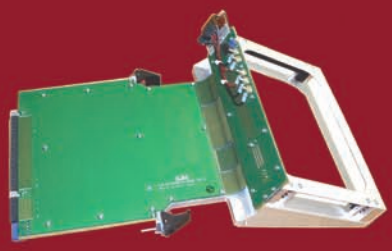
VME64x



VXS (VITA 41)



VPX (VITA 46)



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BOARDS & SYSTEMS ABOVE & BEYOND

Case study: EFV keeps pace with Ethernet to actualize net-centric warfare

By Mike Southworth

The Expeditionary Fighting Vehicle (EFV) planes the water at up 46 km/h (28.58 mph) equipped with an onboard Ethernet network connecting rugged workstations and computing LRUs. Photo courtesy of USMC.

The success of net-centric warfare is dependent on fast, secure communications technology – specifically Ethernet. To meet the military's demands for Ethernet-enabled vehicles, Ethernet switches and routers need to be increasingly rugged and capable of meeting future network requirements. A case study of the USMC's Expeditionary Fighting Vehicle (EFV) with its Tactical Switch Router (TSR) exemplifies this trend.

The advent of net-centric warfare has spurred the rapid development of networking technology as the military's success must rely on the accuracy, power, and speed of communication technology. To ensure the safety of soldiers and mission success, net-centric operations depend on information exchange platforms that support mature and well-tested protocols, offer data in near real time, and provide advanced roadmaps for future performance. Currently the primary communications technology to meet these requirements is Ethernet.

Although not new on the military scene, this venerable COTS LAN technology is replacing a myriad of other backplane choices. Traditional vehicle data buses such as MIL-STD-1553, CANbus, and RS-232 continue to have an important role in mission-critical military applications. However, due to their limited bandwidth and the growing priority to gather and synthesize information as quickly as possible for situational awareness, Ethernet is becoming the preferred enabler for situational awareness in many battlefield platforms.

Despite the desire for high speed and performance, not every application receives tangible benefits from the faster pipe offered by GbE or 10 GbE. In fact, Fast Ethernet often meets current network requirements, since actual Wide Area Network (WAN) backhaul speeds are often slower than 100 Mbps in the field. This is because the speed of *inter*-vehicle communications can be constrained by the wireless connection, which becomes the bottleneck for speed and performance. However, for *intra*-vehicle communications not limited by the bottlenecks of a WAN connection, onboard computing devices certainly benefit from 1 Gbps or faster connectivity.

To help the military meet its current need for Ethernet-enabled vehicles and to anticipate future demands, there is increasing pressure on defense contractors to provide rugged Ethernet switches and routers that meet the requirements of Space, Weight, Power, and Performance – Cooling and Cost (SWaP2-C2). Additionally, these network switches and routers must endure the harshest environments to enhance situational awareness in unmanned aircraft, tactical ground vehicles, and maritime assets, where standard commercial-grade equipment cannot survive. An excellent example of this is the Tactical Switch Router (TSR) found in the USMC's Expeditionary Fighting Vehicle (EFV), as the following case study illustrates.

Expeditionary Fighting Vehicle – Net-centric Ethernet at work

One of the many significant deployments of Ethernet in the military is in the Expeditionary Fighting Vehicle – the Marine Corps' highest-priority ground combat modernization program. Designed and developed by prime contractor General Dynamics, the EFV is an armored amphibious vehicle capable of seamlessly transporting Marines from Naval ships located beyond the visual horizon to inland objectives (see article lead-in photo above). The new vehicle is a self-deploying, high-water-speed, armored, tracked vehicle to provide essential Command, Control, Communications, Computers, and Intelligence (C4I) functions for embarked personnel and other EFV units[1].

General Dynamics initially selected Fast Ethernet as the main inter-vehicle network protocol for linking various IP-enabled computing and communications devices in the EFV. General Dynamics needed a rugged router that wasn't yet commercially available to sustain its networking requirements. General Dynamics contracted with Parvus Corporation to develop the Tactical Switch Router – which enables the deployment of communications-on-the-move and information-sharing capabilities, supporting the Marine Corps' net-centric operations initiatives.

The EFV includes multiple connections for a network backhaul over satellite or line-of-sight wireless technologies, depending on the vehicle variant, to fulfill its mission. Empowering situational

[1] At the time of writing this article, Secretary of Defense Robert Gates had proposed budget reductions for Future Combat Systems vehicles. Although the EFV has come under question, it remains unscathed for now.

awareness, the TSR subsystem connects to a variety of IP-enabled computing workstations and Radio Frequency (RF) device LRUs to support an Ethernet-based intra- and inter-vehicle network. Remote users can exchange voice, video, and data communications with a central site and securely access resources in real time.

Developing the Tactical Switch Router

The miniaturization of components allows more functionality to be packaged into communications technology – a key requirement of the USMC for the TSR. Parvus met this challenge by combining the router and Ethernet switch in one stand-alone Line Replaceable Unit (LRU). This engineering development simplified installation and maintenance for the USMC, which ultimately saves time and reduces costs.

By basing the TSR router on Parvus' COTS DuraMAR Mobile IP router product, the EFV benefited from a small form factor rugged router subsystem that integrated Cisco Systems' Rugged 3200 Series Integrated Services Router (ISR) and Internetwork Operating System (IOS) with an isolated military-grade DC/DC converter in a rugged chassis with MIL-C-38999 interfaces. Capable of delivering secure data, voice, and video communications to stationary and mobile network nodes across wired and wireless networks, this proven IP networking solution includes Cisco's stackable embedded PC/104-*Plus* modules, the 3251 Mobile Access Router Card (MARC), 3201 Fast Ethernet Switch Mobile Interface Card (FESMIC), and 3201 Serial Mobile Interface Card (SMIC) (see Figure 1).

The pervasiveness of Cisco technology and its IOS software in the government arena was a critical factor for specifying this routing technology in the TSR. According to industry reports, Cisco has at least a 70 percent market share in the U.S. government's IP network infrastructure. By including network management software that the U.S. Marine Corps has been trained to operate, the learning curve to operate the TSR would be diminished and improve the EFV's time to deployment.

The 3200 Series is one of the few rugged routers that passed the Common Criteria Evaluation and Validation Scheme (CCEVS) EAL 3 assurance program sponsored by the National Institute of Standards and Technology (NIST) and the National Security Agency (NSA). Further, it is one of the first to support Internet Protocol (IP) mobility per the Internet Engineering Task Force's (IETF's) Mobile IP Standard RFC 2002. With Mobile IP, mobile device users can move from one network to another while maintaining a permanent IP address.

Cisco IOS software also afforded the USMC advanced capabilities for network security, manageability, and scalability. Some of the integrated network security features include authorization and authentication, stateful firewall, intrusion detection, and Triple Digital Encryption Standard (3DES) or Advanced Encryption Standard (AES) encryption for VPNs. Remote management capabilities give network managers visibility into and control over the remote network, including devices connected to the router. Powerful debug and troubleshooting commands allow network managers to quickly

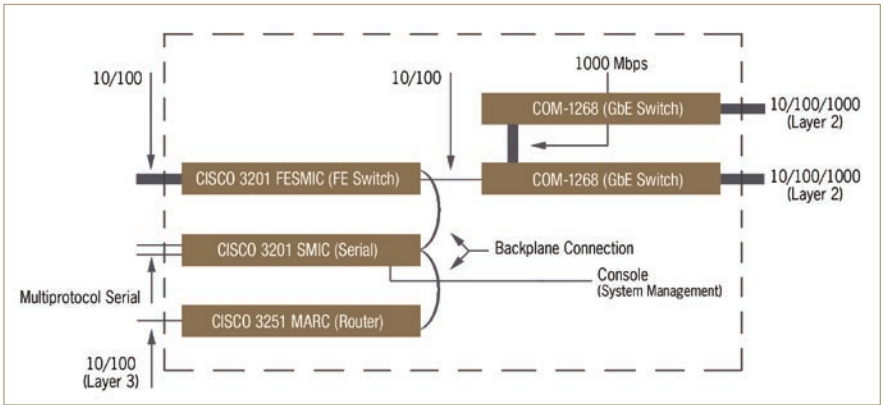

Figure 1 | TSR/DuraMAR 3230 system diagram depicting Cisco 3200 router and serial and Ethernet switch cards interfacing with two Parvus COM-1268 GbE switches.

isolate network problems and securely make changes to network configurations.

Since the EFV is an amphibious vehicle armed with a 40 mm MK44 cannon and 7.62 mm machine gun, the TSR subsystem would be exposed to gunfire shock, as well as underwater and tracked vehicle operation with operational shock levels in excess of 20 *g*s. The rugged 3200 ISR was specifically designed for establishing a highly secure IP network with remote devices in a moving or stationary vehicle in harsh conditions. It also underwent environmental testing to MIL-STD-810F and SAE J1211/J1455 parameters.

Advancing the EFV

As the DoD moves toward upgrading to Internet Protocol version 6 (IPv6) this year, support of IPv6 has become a core requirement for network-centric warfare. Again, the 3200 router was the answer as its IOS management software is IPv6 compliant – further validating the necessity of the 3200 router in the EFV.

In keeping pace with the initiative to "future proof" the EFV, the latest revision of the TSR integrates two PC/104-*Plus* GbE switch cards into a new chassis to provide a total of 17 Ethernet ports – more than triple the number of available ports on the original TSR configuration or normally available from Cisco's standard product. By integrating the 3200 Series' mobile access router technology with PC/104-*Plus* GbE switch cards, the TSR offers expanded LAN port count and consolidated switch and router functions into a single hardened subsystem designed to MIL-STD-810F and MIL-STD-461E environmental conditions. Sealed MIL-C-38999 connectors bring out an IOS-managed 10/100 WAN port, three IOS-managed 10/100 switch ports, and 13 10/100/1000 GbE switch ports, as well as 2 multiprotocol serial ports and an RS-232 management console port. These additions supply the EFV with enough capacity to meet future networking demands.

Since receiving the original TSR development contract in 2007, Parvus has also received additional contracts for reliability improvements and functional upgrades to ensure system performance. Among these improvements were upgrades in ruggedness and thermal design. Flex cabling was instituted to improve shock and vibration

Figure 2 | The EFV program influenced the development of the COTS DuraMAR 3230 subsystem, which has only minor mechanical differences from the TSR and will become a standardized version of the TSR for generalized use by the armed forces.

and provide solid reliability. Conduction cooling advancements were also instituted, such as clamshell heat sinks for each printed circuit card assembly and finned extruded chassis to reduce thermal issues and improve reliability. The latest version of the TSR subsystem helped shape other rugged COTS router product offerings (Figure 2).

Future of Ethernet in net-centric warfare

As the military's growing quantity of complex, mission-critical applications needs increasing ruggedness, security, and bandwidth, GbE is ensured a productive future in net-centric operations. However, the successful implementation of 10 Gigabit speeds depends on the development of switches and routers to accommodate this technology. As witnessed from the design and deployment of EFV and the TSR, government contractors and suppliers are well primed to help the military meet its net-centric objectives.

Mike Southworth *serves as director of marketing for Parvus, a manufacturer of rugged COTS computing and IP networking subsystems for military and aerospace applications. In his role at Parvus, Mike oversees the product management and marketing communications programs. Mike holds an MBA from the University of Utah and a B.A. in Public Relations from Brigham Young University. He can be contacted at msouthworth@parvus.com.*

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Editor's Choice Products

Editor's note: *Military Embedded Systems is "hip" to the whole Web 2.0 social networking revolution. While we don't know which of today's buzzy trends will last, we're going to start including links to vendors' social networks, when provided. You can also reach us on Twitter, Facebook, and LinkedIn ... and that's just for this week. Next week there'll undoubtedly be more new sites.*

Boards warranted for seven years

Ironically, editor Chris Ciufo just purchased an extended warranty for a Subaru Outback for 7 years/70,000 miles. Seems as if Acromag had the same idea for its PMC, Industry Pack, PCI, and CompactPCI boards and modules: Adding six years onto the base one-year warranty gives users a huge confidence boost in Acromag's products. We at *Military Embedded Systems* applaud this move and believe it could very well be the industry's longest warranty. (Let us know if you have any input.) And while we normally only grant *Editor's Choice* awards to *products* – we believe this *service* capability is certainly just as deserving.

The company is able to offer this extended warranty, it says, because of the confidence it has in manufacturing, components engineering, quality, and design. For instance, military-grade components are used where available, ESD is controlled via ANSI/ESD S20.20, and PCBs receive 100 percent in-house inspection *after* they've been purchased to IPC-6012 Class III (Qualification and Performance Specification for Rigid Printed Boards). Build quality is compliant with IPC-A-610 Class II (Acceptability of Electronics Assemblies Training and Certification Program). But there are a couple of caveats: The additional six years requires registration with Acromag, and PMC FPGA modules are only warranted one additional year.

Acromag • www.acromag.com • RSC# 42458

Rugged COTS LCD with built-in image algorithms

Sure, "anyone" can ruggedize an LCD to make it withstand extreme temperatures, shock, vibration, salt spray, and humidity in explosion environments. We're kidding, of course. Ruggedizing an LCD while also making it sunlight readable is no small feat. That's why Z Microsystems' Ground Control Station (GCS) display panel with Real-Time Enhanced Video (RTEV) is so darned compelling. It is designed for the harshest military applications, *and* it has built-in image enhancement electronics. Designed for live video surveillance feeds such as those from UAVs or other sensors, the RTEV guts are based upon FPGA algorithms performing signal processing.

Two primary modes include image enhancement and edge detection algorithms, both of which add minimal latency for real-time operations. Functions include: contrast enhancement during changing brightness and contrast situations; dusk/dawn viewing; "de-hazing" to enhance image readability in fog and sand storm environments; and edge detection to identify anomalous shapes while highlighting details. A Picture-In-Picture (PIP) feed in RGB or NTSC can be scaled or blended into the primary image, and all GCS panel functions can be toggled on or off locally or remotely. This third-generation GCS has updated electronics and is designed for LCD tech refresh, meaning that the internal LCD can be swapped out when newer panels come along.

Z Microsystems • www.zmicro.com/rtev • RSC# 42459

Quad-core rugged enterprise server family

SWaP, RAS, RES: These compose the alphabet soup Themis Computer uses to describe its XR3 family of 1RU, 2RU, and 3RU rugged servers. The Rugged Enterprise Servers (RES) use Intel's Nehalem-inspired quad-core Xeon 5500 CPUs to emphasize SWaP and Reliability, Availability, and Service (RAS). The mission-critical designs are meant for 24/7 operation in land- and sea-based platforms that can withstand 25 *g*, 20 ms, three-axis operating shock, and 3.0 Grms, 8-2,000 Hz operating vibration. Operating temperature of the 20" deep aluminum chassis is from 0 °C to +65 °C.

Bolted to the CPU is up to 96 GB ECC SDRAM (1RU) or 144 GB (2RU and 3RU versions), and up to eight 2.5" lockable and removable HDDs. (Image is of the interior of a 3RU.) Fans are hot swappable, and there are single or redundant power supplies operating at 110/220 VAC or 18-72 VDC. Meanwhile, optional front-panel filters protect the guts from being sandblasted by nasty gritty stuff. As you'd expect, the servers run Linux, Sun Solaris, and flavors of Windows.

Themis Computer • www.themis.com • RSC# 42460

'Modded' memory comes to COTS PCs

PC gamers are famous for "modding" their rigs by overclocking the CPUs to achieve better-than-stock performance. But doing so causes systems to run hot, necessitating beefier fans and liquid cooling. This same technology can also be applied to benign military gear that still needs to operate reliably in hot desert environments. Corsair, a leader in high-performance computer and flash memory products, says its Hydro Series H30 water block and Ice Series T30 thermoelectric coolers are capable of cooling memories *below* room temperature.

The Hydro Series H30 is an anodized aluminum water block capable of cooling up to six Dominator GT (memory) modules using 3/8 tubing to route water or another coolant. For more extreme environments, the thermoelectric Ice Series T30 (shown) uses Peltier technology that can reduce temperature as much as 20 °C below ambient. When both devices are used together, memory can be overclocked by up to 100 MHz. Memory condensation is avoided – thus maintaining reliability – via a sophisticated humidity sensor to prevent DIMMs from being cooled below the chassis' dew point.

Corsair Cooling • www.corsair.com • RSC# 42461

Rugged wearable computer

Looking like the stuff of science fiction, the Ridgeline W200 wearable computer from Glacier Computer is made of a reinforced magnesium alloy with a QVGA 3.5" touch-screen LCD display. Running either Windows CE 6.0 or Linux, the wrist-mounted PC is ideal for some defense applications such as maintenance or always-connected TOC operations. Shaped to the arm's contours and weighing 10.2 ounces with the battery, the 11-key backlit keyboard combines with Wi-Fi (802.11b/g), Bluetooth, and GPS to provide wireless access to services. In addition, remote host access can also be granted via a wired ("docked") connection for secure download or tethered operations.

The Ridgeline W200 is powered by an Intel 400 MHz PXA270 XScale CPU with 128 MB of RAM and 128 MB of NV flash. Included are audio in/out, a USB port, a mini-SD slot, and a hot-swappable battery. The device operates over -10 °C to +50 °C and has a unique feature that drops the unit into low-power mode to save battery energy based upon tilt and silent reckoning physical positions. There's also an integrated stylus for pen-based inputs.

Glacier Computer • www.glaciercomputer.com • RSC# 42462

Clean power, clean design

Military environments are notoriously dirty: Marines scrabbling around in the mud, the grease and bunker oil sloshing around in a bilge, and the floor of an AC-130 gunship littered with spent brass. Oh, and don't forget the power supplies for the electronics, which can experience surges, sags, and frequency shifts plus suffer from extended brownouts. These are the challenges that Falcon Electric's Solid-State Voltage Regulator (SVR) is designed to solve. Available in rack-mount/tower design and operating over 0 °C to +55 °C, the SVR Pro continuously generates "new, ultra-clean AC power" from an input ranging from 80 to 138 VAC at an impressive 0.97 input power factor correction.

The COTS unit is available in 1.5 kVA, 2.2 kVA, and 3 kVA versions – all weighing a mere 31 pounds while supplying a *pure sinewave with ±2 percent voltage regulation.* Difficult, high in-rush currents are easily tamed, as are input harmonics and other power-feed nasties. Based upon microprocessor technology, the onboard LCD displays instantaneous line, load status, and operating parameters. As well, the units are available for 230 V operations at 50 Hz for international operation, and an optional battery backup can provide minutes to hours of uptime.

Falcon Electric
www.falconups.com
RSC# 42267

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Throwing a *Lasko* around serial ports

By Chris A. Ciufo, Editor

According to IDC, the market for Ethernet equipment will grow at a CAGR of 4.2 percent to $3.2 billion over 2008 to 2013. Meanwhile, Gartner reports, "[Ethernet] port shipments will grow at a compound annual rate of 1.8 percent from 2008 to 2013 … Gigabit Ethernet ports will grow to 49.8 percent of total shipments in 2013." These are big numbers representing a growing market – even in a recession. That's because Ethernet is everywhere.

Say, how many of you remember the bulky, fat yellow cables that usually ran above the office ceiling tiles, punctuated by a big silver tap box dropping a smaller cable down to your computer terminal? Show of hands, please? I'll bet not too many of you would raise your hand. That's because Ethernet has evolved considerably since then to a ubiquitous 10/100/1000 Mbps LAN connecting computers – not terminals – via cheap Cat5e and RJ-45 connectors. The speed keeps going up while the cost goes down as tomorrow's 10 GbE paves the way. I am convinced that Ethernet is on the cusp of being more prevalent than was RS-232 in its day, probably even in military applications.

Freescale – then as Motorola – pioneered the idea of packaging high-performance MCUs with Ethernet controllers. From their humble 68xx QUICC devices to PowerPC-based PowerQUICC MCUs and onward to their current generation of 32-bit MCUs with Ethernet, Trusted Platform Module (TPM), encryption, and more – the company continues to out-innovate the competition in exceptionally full-featured, system-level MCUs. And most of them have Ethernet built right in. Who needs serial ports?

In fact, replacing serial connectivity in myriad systems – from SCADA to factory automation and machine vision, to medical and military – is just what Freescale's MCF51CN128 is all about. Though I hate the nomenclature – can't they just stick with its original code name of *Lasko*? – the company combines a V1 32-bit ColdFire MCU[1] with Ethernet, software, and available board-level development system into one of the most comprehensive off-the-shelf and "ready-to-eat" Ethernet systems I've seen to date[2].

From my time in the defense industry, I can attest that serial ports and general-purpose TTL I/O lines are everywhere. What's compelling about *Lasko* (you see, we're now on a first-name basis) is that it aims to bridge those legacy connections to Ethernet and bring bespoke systems onto local LANs or ready them for Internet access. But I'm not talking about the soda machines, point-of-sale terminals, or Remote Telemetry Units (RTUs) that Freescale is envisioning. I'm referring to "disconnected" military equipment scattered about Navy ships being wired with Ethernet backbones via the *Navy Open Architecture* mandate, Army and Air Force command posts that string LANs between PCs but still plug in bulky 38999-equipped boxes housing sensors and radios, and in-vehicle vetronics hull/turret (HEU/TEU) units that could benefit from Ethernet connectivity for more than just maintenance or diagnostics.

Lasko intrigues me greatly because it's designed to be so cheap (sorry, Freescale) that it'll replace serial driver devices with Ethernet. At $2.99 in big volumes, it's hard to believe the thing is stuffed with a 12-channel A/D, 2 UARTs, 2 SPI, 2 I2C, 70 GPIO plus Ethernet, and a 32-bit CPU. The company's included MQX OS also adds a TCP/IP stack, Telnet, SSH and SNMP applications, as well as an embedded and secure Web server so equipment can hang off the LAN all by itself and either be queried or squawk back autonomously. As well, in low-power mode, Lasko sips a mere 500 *nanoAmps*, while using only 50 mA in full mode at 50 MHz (at 3 V).

Deficiencies? Well – Power over Ethernet would be nice, but that's not what Lasko was designed for. There are myriad other members of the MCU family with different flavors if that's your preference – including PowerPC-based MCUs that are equivalent to the IBM-based 440 cores in some Xilinx V-5 FPGAs (just in case code portability is important to you). And since Lasko was designed for industrial apps, it'll work in most wide-temp defense systems, too.

This whole concept of *really cheap and ubiquitous Ethernet in military systems* has personal significance for me, which is why I'm railing on about it. When I was at Dy4 Systems 10 years ago[3] my engineering colleagues thought I was Section 8 when I specified 10 Mb Ethernet on the company's first PowerPC single board computer. "No one will ever use Ethernet in defense," was the conventional wisdom at the time. In fact, Dy4's PPC SBC became hugely successful and took the competition by surprise – partly because of its built-in COTS Ethernet port.

Perhaps Lasko will offer similar market changes by replacing all those serial ports in legacy defense systems. We'll have to wait and see.

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[1] Interestingly, the V1 ColdFire core is also available as IP for Altera's Cyclone III FPGAs. V1 is a simplified version of the 68K-inspired V2 core; for more info, refer to: www.freescale.com/files/pr/coldfirelicensing.html.

[2] I recently moderated an E-cast with Freescale on the topic of Ethernet called "The Ultimate Ethernet Solution: Connect Serial to Ethernet in Seconds!" (See http://ecast.opensystemsmedia.com, then click on Archived – Recent)

[3] Dy4 was acquired by Vista Controls and is now part of Curtiss-Wright Controls Embedded Computing.

MLRS Multiple Launch Rocket System AH-64 Helicopter T-6A Peloton
CV90 Armored Vehicle DDG-1000 Multi-Mission Destroyer Roland Air Defense System
HIMARS Artillery Rocket System B-2 Stealth Bomber F-35 Lightning II
LHD Class Amphibious Assault Ship Expeditionary Fighting Vehicle Gripen Fighter
Littoral Combat Ship A400M Transport NSSN Virginia Class Submarine
F-117 Stealth Fighter MEADS Air Defense System EMB-145 Challenger 2 Tank
M2/M3 Bradley C-5 Transport NH-90 ASW Helicopter AH-1W Helicopter
Predator RQ-1 E-2C/D Early Warning Aircraft Neuron UCAV V-22 Osprey

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